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A Study of NBTI and PBTI (Charge Trapping) in High k Stacks with NiSi, TiN, Re Gates

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Abstract: Threshold voltage (V_t) of a field effect transistor (FET) is observed to shift with stressing time and this stress induced V_t shift is an important transistor reliability issue. V_t shifts that occur under negative gate bias is referred as NBTI and those that occur under positive bias is referred as PBTI or charge trapping. In this paper, we present results of experimental and modeling studies of NBTI and PBTI for a variety of FETs with different gate dielectric stacks (SiO_2/HfO_2, SiON) and gate materials (TiN, NiSi, Re, poly Si). In part I**,** NBTI measurement and modeling results for SiO_2/HfO_2/metal pFETs are presented. The main result is that the estimated V_t shifts at 10 years due to NBTI is independent of metal gate material and is comparable to those for conventional SiON/poly-Si pFETs. In part II, PBTI measurement and modeling results for SiO_2/HfO_2/metal nFETs are presented. The main results are as follows. PBTI significantly increases as the Hf content in the high κ layer is increased. PBTI in TiN and Re gated SiO_2/HfO_2 devices is much smaller than those observed for SiO_2/HfO_2/NiSi. In summary for SiO_2/HfO_2 stacks, NBTI is observed to be independent of gate material whereas PBTI is significantly worse for FUSI gated devices. Consequently, HfO_2 FETs with TiN and Re gates exhibit over all superior transistor reliability characteristics in comparison to HfO_2/FUSI FETs.

Experimental Details: NBTI and PBTI measurements were made on pFETs and nFETs, respectively; the details for measuring V_t shifts (ΔV_t) as a function of stress time is given elsewhere [1, 2]. ΔV_t measurements were made at 125°C at various positive and negative stress voltages. In this study, all the high κ stacks consist of SiO_2 (~6Å)/HfO_2 (25Å) and received a high temperature (~1000°C) post deposition anneal and a forming gas anneal. TiN and Re gates were deposited by sputtering and CVD, respectively. Silicidation temperature for NiSi was 500°C.

NBTI Modeling and Experimental Study: Measured ΔV_t versus stress time curves are analyzed by using previously proposed model for NBTI [1]. The model assumes that both interfacial and oxide hole traps are created due to depassivation of Si-H bonds at the silicon interface, and the depassivation is mediated by dispersive diffusion of protons. The equilibrium hole occupancy of traps is given by Fermi function. The model predicts a stretched exponential equation for V_t shift as a function of stressing time (t) as given below.

$$|\Delta V_t(t)| = \Delta V_{max} \cdot (1 - \exp - (t/\tau_o)^{\beta}) \qquad (1)$$

where ΔV_{max}, τ_o and β are fitting parameters; τ_o and ΔV_{max} are both function of stress oxide field E_{stress}, whereas β is independent of E_{stress}. Equation 1 will be used for fitting ΔV_t versus stress time curves for NBTI, thus estimating ΔV_t values at 10 years lifetime.

Fig**.** 1 (a) - (d) shows the dependence of NBTI induced ΔV_t on stress time at various negative stress voltages for a variety of pFETs. As shown in Fig. 1, the model fits (eq. 1) are in good agreement with data for a variety of pFETs and are used for estimating ΔV_t at 10 years of stress time. In Fig. 2, NBTI results for NiSi, TiN and Re gated pFETs are compared with those conventional pFETs. Since T_{inv} values are different for various pFETs, ΔQ_{max} values are compared. ΔQ_{max} is the charge density created after 10 years of stress: $\Delta Q_{max} = \Delta V_t$ (10 yr) $\cdot \varepsilon_{ox}/T_{inv}$, where ε_{ox} is the permittivity of SiO_2 and ΔV_t (10 yr.) is the estimated shift after 10 years of stressing and are estimated by fitting equation 1 to measured curves as shown in figures 1**.** In Fig. 2, NBTI induced ΔQ_{max} for TiN and Re pFETs are observed to be comparable to those for NiSi and convention pFETs. Since all the pFETs in this study have a similar Si/oxide interface, the result of Fig. 2 indicates that NBTI depends predominantly on the Si/oxide interfacial property. In summary, NBTI shows no measurable dependence on gate material or dielectric stack provided Si/oxide interfacial quality remains same.

PBTI Modeling and Experimental Study: A model for charge trapping is proposed for high κ nFETs [2]. The trapping physics in high κ stacks is assumed to be same as that were proposed for SiO_2 with one main exception: the trapping cross section is assumed have a small distribution in its values. Like the NBTI model equation, the model equation for charge trapping is also a stretched exponential equation as shown below.

$$\Delta V_t(t) = \Delta V_{max} \cdot (1 - \exp - (t/\tau)^{\gamma}) \qquad (2)$$

where ΔV_{max}, τ and γ are fitting parameters. Equation 2 will be used for fitting ΔV_t versus stress time curves for PBTI, thus estimating ΔV_t values at 10 years lifetime.

Fig. 3 shows the dependence of PBTI on stressing time and bias for SiO_2/HfO_2/NiSi, SiO_2/HfSO/NiSi and SiO_2/NiSi nFETs. From Fig. 3, we observe that the charge trapping increases as the Hf content in the high κ layer increases, thereby indicating that the interaction between poly-Si (before silicidation) and Hf plays an important role in creating traps in the high κ gate dielectric stacks. Fig. 4 shows the dependence of PBTI induced ΔV_t on stress time for SiO_2/HfO_2/TiN nFETs. In both figures 3 and 4 symbols are measurements and solid lines are model fits obtained using equation 2. As shown in these two figures model equation gives good fits over several decades of stress time for a variety of high κ nFETs. Measurements similar to those for HfO_2/TiN nFETs were also made for HfO_2/Re nFETs. In Fig. 5, PBTI in HfO_2 stacks with TiN and Re as gates are compared with those for HfO_2/NiSi nFETs. As shown in the figure, PBTI in NiSi gated nFETs is significantly worse than PBTI in TiN and Re gated devices.

Conclusions: Experimental and modeling study for a variety of high κ FETS is presented. NBTI and PBTI in FUSI (NiSi), TiN,

and Re gated HfO_2 devices are compared: NBTI is independent of gate material and is comparable to conventional SiON/poly-Si FETs. PBTI is worse for HfO_2/NiSi nFETs in comparison to HfO_2/TiN and HfO_2/Re devices. Consequently, HfO_2 FETs with TiN and Re gates exhibit superior V_t reliability in comparison to HfO_2/NiSi FETs.

Reference:

[1] S. Zafar, JAP (2005);
[2] S. Zafar et al, JAP 93, 9298 (2003)

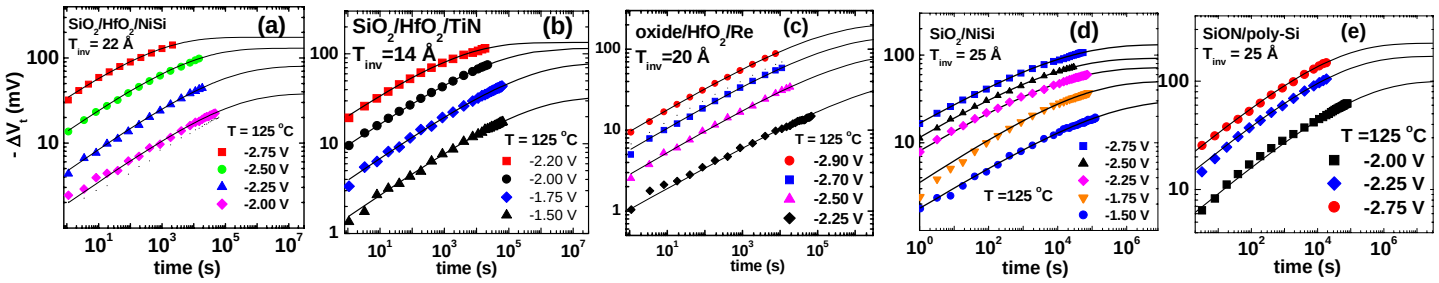

Fig 1: Dependence of NBTI induced V_t shift for various pFETs :**(a)** SiO_2/HfO_2/NiSi, **(b)** SiO_2/HfO_2/TiN, **(c)** SiO_2/HfO_2/Re, **(d)** SiO_2/NiSi, and **(e)** SiON (~5%N)/poly-Si; symbols are measurements and solid lines are model fits using eq. 1.

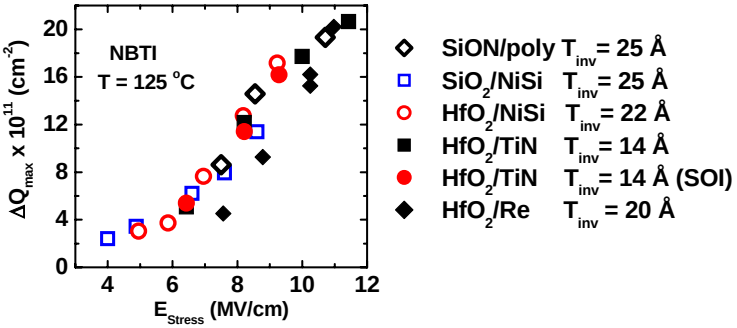

Fig. 2: NBTI comparison for SiO_2/HfO_2 pFETs with FUSI (NiSi), TiN and Re gates; ΔQ_{max} is charge density created after 10 yrs of stressing and is estimated from fits shown in Fig. 1 and 6. NBTI is similar for HfO_2 pFETS with different gate materials (NiSi, TiN, Re) & comparable to SiON/poly pFETs.

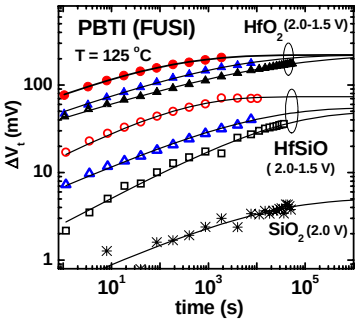

Fig. 3: PBTI for NiSi gated nFETs with SiO_2, SiO_2/HfSiO & SiO_2/HfO_2 as gate dielectrics; symbols are measurements and solid lines model fits using eq. 2. PBTI becomes worse with increasing Hf content in the dielectric layer.

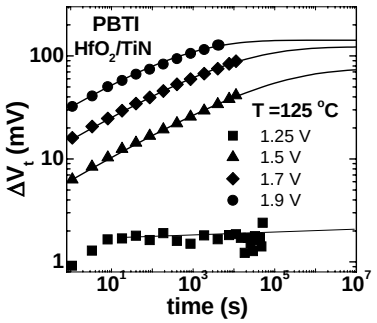

Fig. 4: Charge trapping induced ΔV_t curves for SiO_2/HfO_2/TiN nFETs; symbols are measurements and solid lines are fits using eq.2.

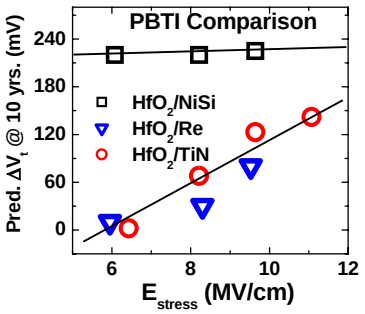

Fig. 5: PBTI comparison for SiO_2/HfO_2 stacks with different gate materials; symbols are measurements. PBTI is worse in HfO_2/NiSi compared