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Comprehensive Understanding of PBTI and NBTI reliability of High-k / Metal Gate Stacks with EOT Scaling to sub-1nm

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Abstract

We have established the comprehensive understanging of PBTI and NBTI reliability of high-k/metal gate stacks. When discussing PBTI, it exhibits a universal relationship in terms of fast transient carrier traps and stress voltage due to the positive oxygen vacancies formation. Using metal gate for Tinv scaling is promising for those improving drain current without PBTI lifetime degradation. However, in the case of NBTI, interface state degradation becomes more serious with Tinv scaling. Thus, high quality interfacial layer, such as wet oxide interface, is promising for improvement of NBTI lifetime.

Introduction

One of the most serious problems for Hf-based gate dielectrics is the BTI life time and the impact of the metal gate on the BTI characteristics has not been clarified so far. Although some studies have been reported on the BTI characteristics of high-k/metal gate stacks [1,2], the mechanism is open to question and guidelines for EOT scaling and improvement have not been formalized. We have already established high carrier mobility $TaSi_x$/HfSiON gate stack [3]. We have investigated the PBTI and NBTI characteristics of these devices in detail, comparing them with poly-Si gate and examining the relationship of the BTI characteristics and EOT scaling to sub-1nm.

Experimental

The sample fabrication process is shown in Fig.1. Interface SiO_2 layers were formed with O_3 or wet oxide. $TaSi_x$/TaSiN/W stacked-metal electrodes were deposited sequentially by PVD. TEM images of the structure are shown in Fig.2. Fig.3 shows the CV curve of an nMOS device with a $TaSi_x$ gate. The values of Vfb are independent of EOT, and no gate depletion layers were observed. PBTI and NBTI were measured at 30-125^{o}C. A charge-pumping technique was applied in order to measure the interface state density. Table 1 shows the conditions used for the samples and the respective EOT values (using NCSU CVC) that were used in our measurements.

Results and Discussion

Differences between PBTI and NBTI

To clarify the Id degradation mechanism, we have separated the effect of ΔVth due to charge trapping and degradation of transconductance (Gm_max). Those mechanisms are quite different between PBTI and NBTI. Although a shift in Vth was observed in the case of PBTI, no degradation of Gm_max was observed. On the other hand, in the case of NBTI, not only was Vth shift observed, but also the degradation of Gm_max, as shown in Fig.4. Fig.5 shows the time evolution of the interface states (Nit) for NBTI and PBTI. Although the values of Nit for PBTI are almost constant, those for NBTI gradually increased. (Sample C) This means that interface trapping occurs near the valence-band maximum of Si. The temperature dependencies are also quite different between PBTI and NBTI. With power law analysis ($\Delta Vth=\alpha \cdot t^{\beta}$), the values of β increase in the case of PBTI, while on the other hand, the values of α increased with increasing temperature and its activation energy was 0.07eV (Fig.6, 7).

PBTI characteristics

In the case of PBTI, only the Vth shift due to charge trapping should be considered. After only 1 sec. of stress, the values of Vth were shifted due to fast transient carrier traps (FTC), and a gradual shift was also observed (Fig.6(a)). Fig.8 shows the calculated values of Ln(α) as a function of stress voltage (|Vg-Vth|). This shows a universal relationship, without regard to the electrode or the EOT, meaning that the quantum state of the FTC depends on |Vg-Vth| and is independent of the kind of gate electrode used and the film thickness. ΔVth is described as ; $\Delta V_{th}=Q\langle x\rangle/\varepsilon_o\varepsilon_{ox}$. (<x>: charge center) Electron trapping is thought to be related to positive oxygen vacancies (Vo^{2+}) [2,4]. Reported neutral oxygen vacancy (Vo^0) level is located lower than Vo^{2+} [2] (Fig.9(a)). For a Vo^0 to be positively charged, an electron must be transferred from HfSiON to the gate electrode by positive stress voltage. At the moment the gate bias stress is applied, only neighboring electrons to the interface can be transferred to the gate electrode, and consequently the Vo^0 become positively charged. This means that <*x*> exists extremely near to the interface between the gate electrode and the gate insulator (Fig.9(b)). Consequently, the value of *Q* only depends on |Vg-Vth|. With increasing stress time, trapping and de-trapping reactions occur continuously, and the Vo^{2+} have spread to the Si substrate direction and charged centers gradually shifted to the center of the gate dielectrics, as shown in Fig.9(c). Consequently Vth have continued to shift with stress time. From these investigations, we concluded that PBTI problem can be discussed by the same manner for both poly-Si and metal gates. Thus we can enjoy improved drain current by Tinv-scaled metal gate without PBTI lifetime degradation.

NBTI characteristics

In the case of NBTI, effects of Nit degradation and charge trapping should be considered separately. First, we will discuss Gm_max degradation due to Nit. Fig.10 shows the time evolution of Gm_max for NBTI in the cases of samples A, B and C ($TaSi_x$ gate, Vg=-2V, 125^{o}C). With decreasing EOT, the degradations in Gm_max were accelerated. NBTI reliability becomes more serious with EOT scaling. Gm_max degradation were related to the Nit as mentioned. For the same stress voltage, the effective electric field in the inversion layer was increased with the $TaSi_x$ gate due to the suppression of the gate depletion layer, consequently hole wave functions (Ψ) distribution in the triangle potential approach to the interface between HfSiON and Si-substrate. As a result, the interface state sensitivity was increased (Fig.11). Then, we will discuss charge trapping phenomena. With power law analysis, values of α were pushed up with increasing temperature as mentioned (Fig.7(a)). This means that the fast-transient hole trapping sites were thermally active. Fig.12 shows the gate leakage current as a function of gate bias for pMOS with carrier separation. Although the hole currents are not thermally active (Ea=0.02eV), the electron currents are thermally active with activation energies (Ea=0.07eV) similar to those of the FTC sites (Fig.7(a)). The hole-trapping sites are thought to be related to negative interstitial oxygen (O_i^{2-}) which are generated as a frenkel-pair of Vo^{2+} [4]. In the case of negative bias, electrons should be transferred toward the Si-substrate from HfSiON beyond the SiO_2 interface layer, as shown in Fig.13. The increase in the trap-sites is thought to be related with the formation of O_i^{2-} by electron current towards substrate. Thus, the suppression of electron current by high quality interfacial layer is a possible guideline for NBTI improvement. If the SiO_2 interface is formed with a high quality wet oxide, hole trapping is dramatically reduced as expected (Fig.14).

Fig.15 shows the BTI lifetime (ΔId 10%) as a function of Tinv. In case of PBTI, since Tinv scaling brings about the reduction of carrier traps, it shows positive trend for Tinv scaling. In case of NBTI lifetime, it becomes more serious with Tinv scaling. For NBTI improvement, to use high quality interfacial layer, which is expected to reduce interface state degradation and hole traps generation simultaneously.

Conclusion

Based on the microscopic understanding on oxygen-related defect in HfSiON film, we have clarified the guideline of BTI reliability of metal gate/HfSiON gate stack. In the case of PBTI for TaSi gates, the mechanism is the same as that for poly-Si gate electrodes even with sub-1nm EOT. In the case of NBTI, the interface state density becomes more important with EOT scaling and the use of metal gates. The improvement of the interface state is promising for longer NBTI lifetime.

References

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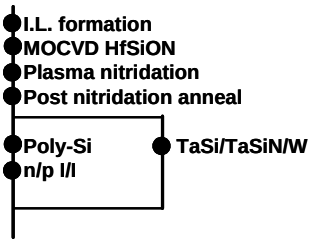


Fig.1 Fabrication flow of a MOSFET with a HfSiON gate film and a metal gate.

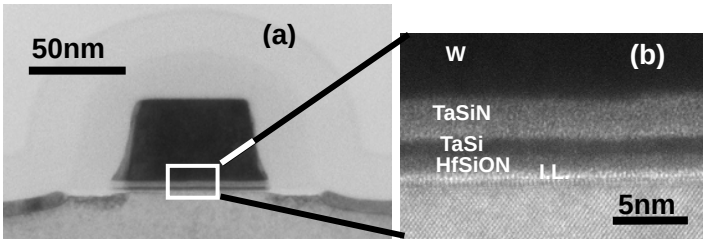


Fig.2 TEM images of full metal gate MOSFET. (a) shows an nMOSFET with L=50nm. (b) shows a the high magnification image around the gate stacks.(HfSiON/TaSi/TaSiN/W=2/2/3.5/50nm)

	HfSiON (nm)	Electrode	EOT (nm)
A	2	$TaSi_x$	0.95
B	2.5	$TaSi_x$	1.24
B'		Poly-Si	1.34
C	3	$TaSi_x$	1.43
C'		Poly-Si	1.53

Table1 Sample conditions of HfSiON thickness, kind of gate electrode and EOTs.

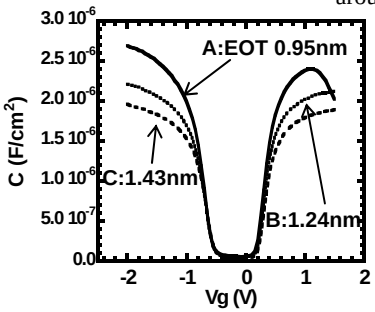


Fig.3 CV characteristics of nMOS with a TaSi gate.

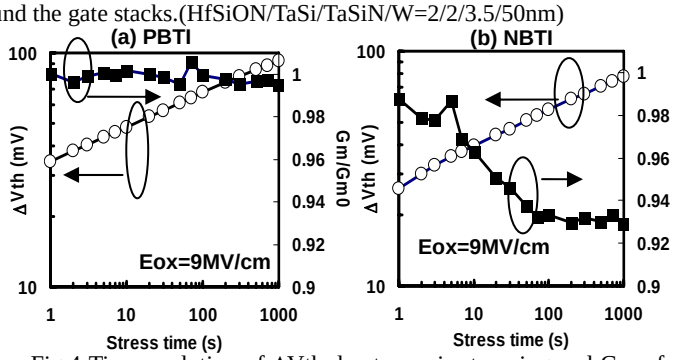


Fig.4 Time evolution of ΔVth due to carrier trapping and Gm of PBTI ((a)) and NBTI ((b)) of Sample C. (W/L=10/1μm, Vd=50mV Eox=9MV/cm, 125°C)

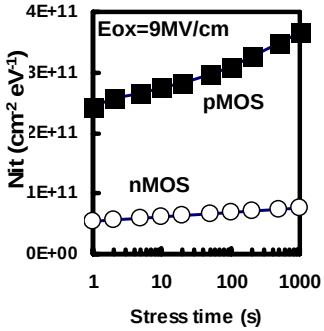
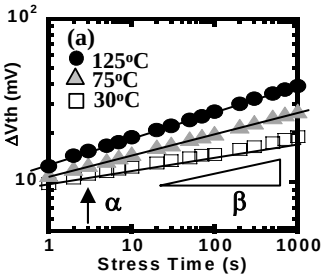


Fig.5 Time evolution of Nit for pMOS and for nMOS.



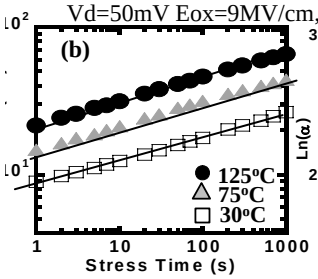


Fig.6 BTI temperature dependence
(a)PBTI (Sample A, Vg=1.8V, T=30,75, 125 °C)
(b)NBTI (Sample A, Vg=-2V, T=30,75, 125 °C)

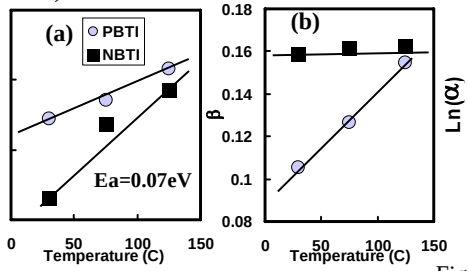


Fig.7 Calculated α((a)) and β ((b))as a function of temperature.

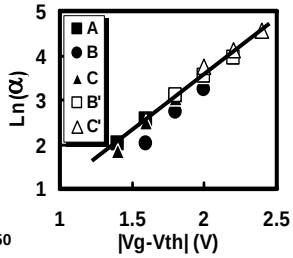


Fig.8 Calculated Ln(α) with power law analysis as a function of |Vg-Vth|.

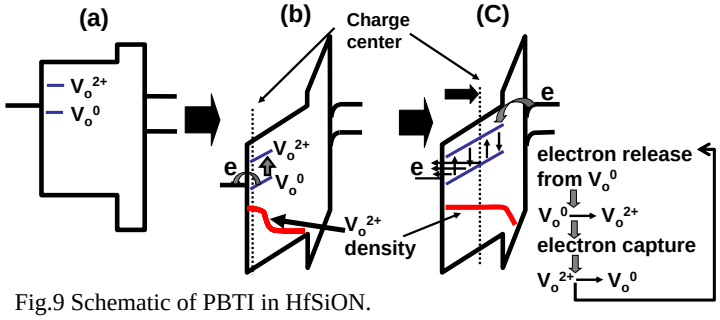


Fig.9 Schematic of PBTI in HfSiON.
(a) Flat band condition. (b)At the moment of applied stress voltage. (Vo^{2+} formation at the interface.) (c)Process of PBTI degradation. (Vo^{2+} increase and charge center shift)

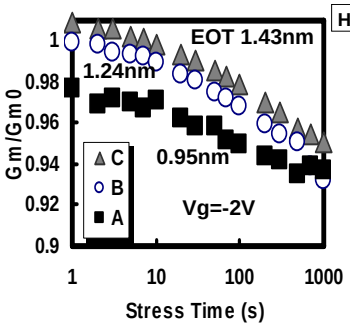


Fig.10 Time evolution of Gm_max degradation with TaSix gate for NBTI.

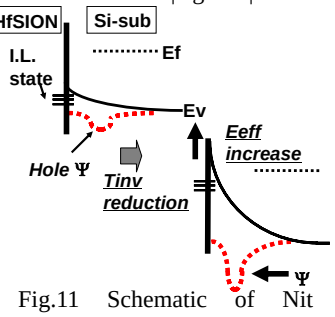


Fig.11 Schematic of Nit degradation with Tinv scaling. Hole wave function approach to I.L. due to Eeff increase.

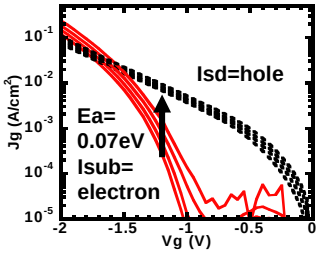


Fig.12 Carrier-separated gate leakage current for pMOS with TaSi gate of (A).

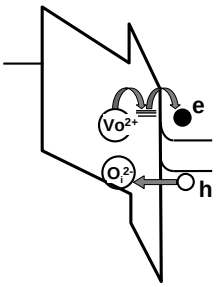


Fig.13 Schematic of NBTI. To generate Oi^{2-} (hole traps) electrons should transfer to the Si substrate.

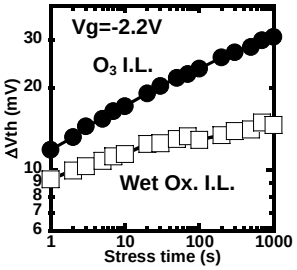


Fig.14 Time evolution of NBTI with O_3I.L. and wet ox. I.L.

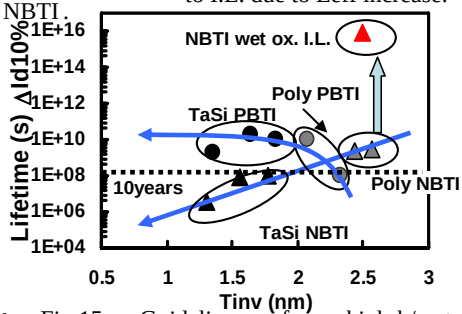


Fig.15 Guidelines for high-k/metal CMOSFET scaling in the point of BTI lifetime. Wet ox. I.L. shows dramatic improvement for NBTI lifetime