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Performance and Reliability Improvement by Optimized Nitrogen Content of TaSiNx Metal Gate in Metal/HfSiON nFETs

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1. Introduction

Metal/high-k gate stacks are very promising gate structures for the 45nm node and beyond. To obtain low V_{th} with Hf based high-k gate dielectrics, the effective work function (WF) of the metal must be near the Si band edge. Because of its suitable WF, TaSi(N) is a potential gate material for metal/high-k nFETs [1]. It is easy to understand that the amount of nitrogen in the gate has significant impact on the performance. The increased nitrogen shifts V_{th} more positive, increases the electron resistivity (ρ), and reduces the electron mobility (μ_{eff}) [1-4]. Nonetheless, the impact of nitrogen in the gate on reliability has not been clarified.

In this paper, we discuss the impact of the nitrogen in TaSi(N) gates on reliability. Moreover, we have successfully optimized the composition of the nFET gate electrode in terms of positive bias temperature instability (PBTI), time dependent dielectric breakdown (TDDB), and μ_{eff}.

2. Experiment

We prepared nFETs with TaSi(N) electrodes with various amounts of nitrogen on HfSiON gate dielectrics as shown in figure 1. HfSiON gate dielectrics with an EOT of 1.0nm were formed using a process developed by us consisting of plasma nitridation followed by high temperature post nitridation annealing [5]. 10nm thick TaSiNx ([N] = 0, 20, 41%) gates were deposited by PVD. For the TaSi ([N] = 0%) electrode, we prepared a 7nm TaSiN / 3nm TaSi stacked electrode as shown in figure 2 (a) (TEM image) to remove the influence of nitrogen diffusion from the SiN hard mask [3]. After patterning the gate electrode, a conventional CMOS flow with S/D spike annealing at 1000°C was carried out.

The composition of the TaSiN electrodes was measured by Rutherford Backscattering Spectrometry (RBS) and the electrode specific resistivity (ρ) was measured by a sheet resistance measurement. The J_g, TDDB, and PBTI measurements were carried out at 125°C.

3. Result and Discussion

Threshold Voltage and Electrode resistivity

Figure 3 shows V_{th} and ρ at 25°C. As the amount of nitrogen in the gate increases, the WF of TaSi(N) shifts to higher values and ρ increases rapidly. Considering the need for low V_{th} and low ρ, the amount of nitrogen should be decreased.

Gate Leakage Current

Figure 4 shows the J_g of various gate materials as a function of the overdrive voltage (V_g - V_{th}) and figure 5 shows schematic band diagrams of the gate structure. As shown in fig.4 (a), all the samples have almost identical levels of J_g in inversion. Since the barrier height at the SiO_2/Si interface for electrons in the substrate conduction band (ΔE_C) is the same for all the electrodes, J_g is expected to depend only on the overdrive voltage. On the other hand, although the dominant carriers in accumulation are holes from the substrate valence band [6], J_g in accumulation is increased by using a TaSi gate. As described later, the use of a TaSi gate increases the number of electron trapping sites. It seems that the trapped electrons intensify the electrical field of the base SiO_2, resulting in an increase in hole current, as shown in fig.5 (b-1).

PBTI and TDDB lifetime

Figure 6 shows the PBTI lifetime (ΔV_{th} = 30mV) as a function of stress voltage (V_g). The PBTI lifetime of the TaSi sample is lower than that of the TaSiN samples, and is less than 10 years even at V_g = 1V. The use of a TaSi gate increases the electron trapping sites, which can be prevented by incorporating nitrogen.

Figure 7 shows the TDDB lifetime of TaSi(N)/HfSiON gate stacks with various amounts of nitrogen in the electrode. Figure 8 shows the charge to breakdown (Q_{BD}) at the 63.6% failure rate. As shown in figures 7 and 8, the TaSi sample has lower TDDB and Q_{BD} lifetimes compared to the TaSiN samples in both inversion and accumulation. Using a TaSi gate not only increases the number of electron trapping sites but also degrades the insulation characteristics. Considering the necessity for high PBTI and TDDB lifetimes, nitrogen should be incorporated into the gate.

Electron Mobility

Figure 9 shows the dependence of μ_{eff} on the effective electrical field (E_{eff}) of TaSi and TaSiN gate nFETs. μ_{eff} decreases with large amounts of nitrogen in the TaSiN gate. However, the highest mobility was obtained with a nitrogen composition of 20%. The low amount of nitrogen in the TaSiN gate decreased the plasma nitridation of HfSiON during gate deposition reducing the number of electron trapping sites.

4. Conclusion

The impact on performance of the amount of nitrogen in the TaSiN electrode of a TaSi(N)/HfSiON gate structure is clarified in Table I. Small amounts of nitrogen achieve low V_{th} and low ρ. However, the TaSi sample shows a higher J_g in accumulation, lower PBTI lifetime, and lower TDDB lifetime than the TaSiN samples. The lowest amount of nitrogen in the TaSiN (in this case [N] = 20%) provides the best performance for TaSi(N)/HfSiON gate stack nFETs with high μ_{eff}, high PBTI and TDDB lifetime.

Acknowledgement

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References

[1] H. C. Wen et al., Symp. on VLSI Tech., 2005, pp. 46-47.
[2] Y. S. Suh et al., EDL.Vol. 24, No. 7, July 2003, pp. 439-441.
[3] S.Inumiya et al., ECS Trans., Vol. 6, Issue 3, 2007, p. 621.
[4] C. S. Kang et al., JVST, B 21(5), Sep/Oct 2003, pp. 2026-2028
[5] S.Inumiya et al., IEDM. Tech. Digest, 2005, pp. 27-30.
[6] M. Sato et al., SSDM, 2005, pp. 26-27.

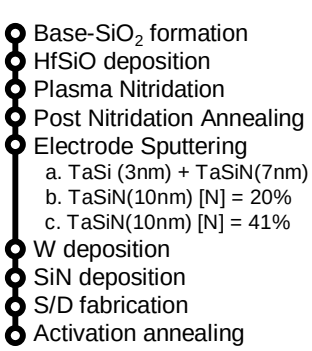

Figure 1. Process flow for preparation of TaSi(N)/HfSiON FETs

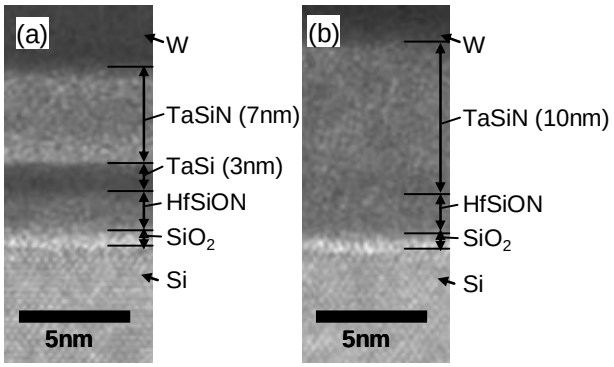

Figure 2. TEM images of (a) TaSiN (7nm) /TaSi (3nm)/HfSiON gate stack and (b) TaSiN (10nm)/HfSiON gate stack.

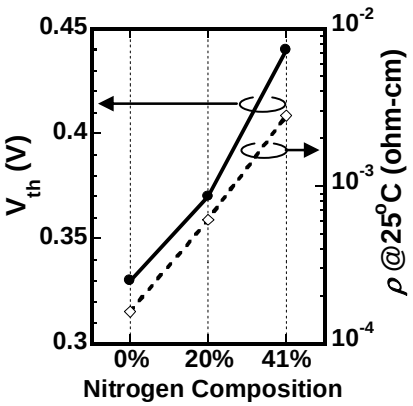

Figure 3. Dependence of V_{th} and ρ on nitrogen composition.

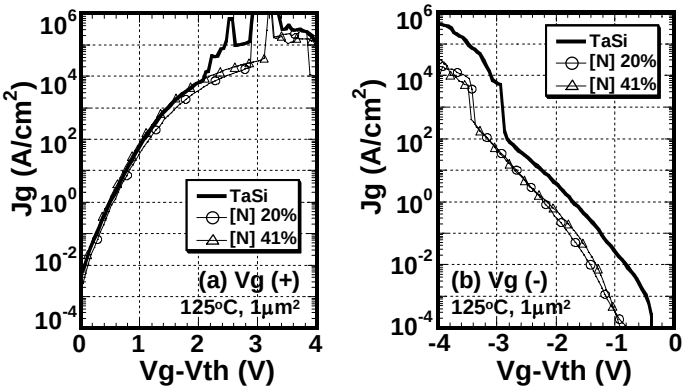

Figure 4. Gate leakage current density of various electrodes in (a) inversion and (b) accumulation.

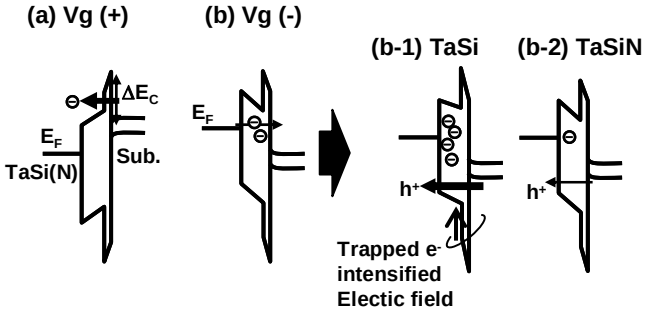

Figure 5. Schematic band diagrams of TaSi(N) /HfSiON gate stacks in (a) inversion and (b) accumulation. Use of a TaSi gate (b-1) increases the number of electron trapping sites and the trapped electrons intensify the electric field of SiO_2, resulting in an increase in hole current.

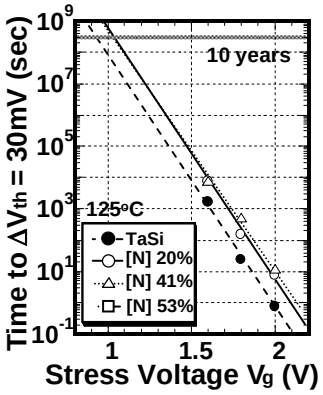

Figure6. Shift in V_{th} as a result of V_g(+) stress (PBTI) for TaSi(N)/HfSiON gate stacks.

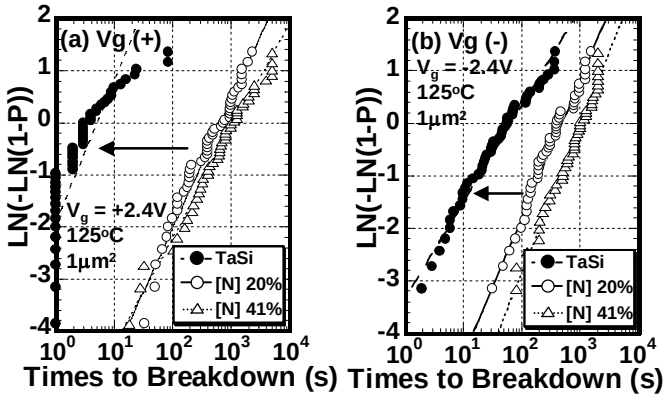

Figure 7. Electrode dependence of TDDB Weibull plots for TaSi(N) /HfSiON gate stacks in (a) inversion and (b) accumulation.

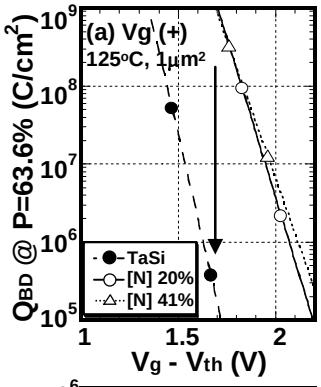

Figure 8. Charge to breakdown of TaSi(N)/HfSiON gate stacks in (a) inversion and (b) accumulation.

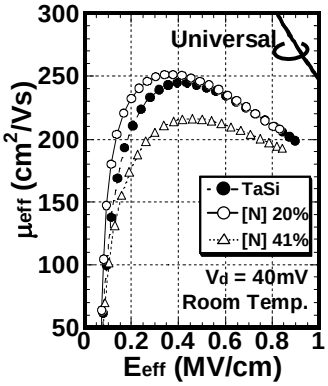

Figure9. The dependence of μ_{eff} on E_{eff} for TaSi(N)/HfSiON gate stacks.

[N]	V_{th} (V)	ρ (Ωcm)	J_g		PBTI lifetime (ΔV_{th} = 30mV) @ V_g = 1V	Q_{BD} lifetime (C/cm²)		μeff @ 0.5MV (cm²/Vs)
			V_g-V_{th} = +1V	V_g-V_{th} = -1V		V_g-V_{th} = +1V	V_g-V_{th} = -2V	
0%	0.33	1.6×10^{-4}	~ 10^{3}	~ 10^{-2}	~ 3 years	~ 10^{13}	~ 10^{7}	~240
20%	0.37	6.1×10^{-4}		~ 10^{-4}	~ 30 years	~ 10^{15}	~ 10^{8}	~245
41%	0.43	2.8×10^{-3}						~215

Table I. The influences of the amount of nitrogen in the gate on the performance of TaSi(N)/HfSiON gate stack nFETs.