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$Si_{1-x}Ge_x$/Si Selective Etch with HCl for Thin Si-Channel Transistors Integration

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1. Introduction

Selective etch of $Si_{1-x}Ge_x$ alloys versus Si has evidenced a lot of applications in microelectronics for the formation of thin Si-channel transistors such as silicon-on-nothing (SON)[1] or multi-gate (MG)[2][3] devices. In a previous paper[4], we published a detailed study of the lateral etch kinetics of $Si_{1-x}Ge_x$ alloys and the obtained morphologies after lateral etching with the HCl/H_2 gas mixture on rotated substrates (etch along <100> directions). We showed that high etching selectivities (>100) were achieved by etching $Si_{1-x}Ge_x$ layers with x=0.30 at low temperatures (<650°C). In the following, we will report similar experiments on non-rotated substrates (etch along <110> directions) for SiGe layers with Ge content above 30% up to 45%. After some morphological considerations, lateral etch kinetics of $Si_{1-x}Ge_x$ alloys were measured as a function of the Ge content and thickness for two different HCl partial pressures. Finally, all these experiments permitted us to determine the more appropriate etching conditions to elaborate double-gates (DG) structures with high-K and metal gate which exhibit excellent performances in term of I_{on}/I_{off}.

2. Experimental details

To conduct the etching experiments, we used an ASM Epsilon 3200 rapid-thermal chemical vapour deposition (RT-CVD) epitaxy reactor. Such a tool, routinely used to deposit Si or SiGe epitaxial layers is equipped with gaseous HCl and H_2 is the carrier gas. Prior to any etching process, $Si_{1-x}Ge_x$/Si stacks were grown on conventional 300mm (100)-oriented substrates and patterned in a way that allowed lateral access to the different $Si_{1-x}Ge_x$ layers. As the HCl etch process exhibits a quasi infinite selectivity against dielectrics, a 20nm SiN layer deposited on top of the stacks was used as a reference. Then, these $Si_{1-x}Ge_x$/Si stacks were submitted to HCl etch and SEM cross-section morphological observation allowed us to extract the different etch kinetics for various SiGe alloys as a function of both Ge concentration and layer thickness.

3. Results

Morphologies

Concerning the resulting morphologies after HCl treatment, the appearance of facets at the tunnel entrance was pointed out previously[4][5]. Their extension depends on the following main parameters: process time, etching temperature and HCl partial pressure. Clearly, these facets are very pronounced at high temperature and low HCl partial pressure, as we can see in Figure 1.a for P_{HCl}=95Torr. They become less extended as the temperature decreases down to 575°C. At higher pressure, i.e. P_{HCl}=555Torr, these facets are no more visible in the whole temperature range: 650°C-575°C (Figure 1.b).

Lateral etch kinetics – Activation Energies

SEM cross-section observations permitted us to extract the lateral etch kinetics of $Si_{1-x}Ge_x$ alloys along the <110> directions with 0.30<x<0.45, between 650°C and 575°C. This way, we found that apparent activation energies increased as the Ge concentration decreased, in the range 37.5 - 45.4 kcal/mol and 46.9 - 53 kcal/mol, for P_{HCl}=95Torr and P_{HCl}=555Torr, respectively (cf. inserts in Figure 2-a and 2-b).

Etch kinetics as a function of the SiGe layer thickness

In order to check the limitations of the vapour-phase HCl etch process in term of SiGe layer thickness, we performed lateral etching on SiGe films with various thicknesses. Therefore, the lateral etch rates have been extracted as a function of the layer thickness from 5nm to 30nm, at 600°C and P_{HCl}=555Torr, and for x=0.35, 0.40, and 0.45 (Figure 3). As the layer thickness is decreased, the etch rate is dramatically reduced but acceptable etch rates are maintained even for SiGe thicknesses down to 5nm. In addition, when the thickness increases, the etch rate tends to saturate for the two higher Ge content layers, i.e. at x=0.40 and x=0.45 (Figure 4).

4. Application on Double Gate devices

Finally, we performed SiGe selective etch with the HCl/H_2 gas mixture on double-gates (DG) devices, with an optimized process. SEM cross-section observations of a DG structure along the gate length and gate width are shown in Figure 5-a and 5-b, respectively. We checked that the SiGe layers (top and bottom) were totally removed along the gate width direction leaving empty spaces on both sides of the thin 15nm Si channel (Figure 5). Due to excellent channel interface, good crystal quality after HCl etch process, and an optimized architecture with high-K and metal gate (Figure 6), DG devices exhibiting high drive currents (2230/1000µA/µm for N/P MOS at V_d=1.2V) and low off-state currents (3/4nA/µm) were achieved[6] (Figure 7).

5. Conclusions

A promising technique for selectively removing SiGe alloys against Si with the HCl/H_2 gas mixture has been presented here. First, morphological considerations permitted us to point out the appropriate conditions for suppressing the appearance of the facets at the tunnel entrance. The lateral etch kinetics were also measured as a function of $Si_{1-x}Ge_x$ layers thicknesses and composition, and the different apparent activation energies at P_{HCl}=95Torr and P_{HCl}=555Torr were also extracted. Finally, thanks to these studies, HCl etch process was implemented on DG devices which exhibit outstanding I_{on}/I_{off} compromises.

References

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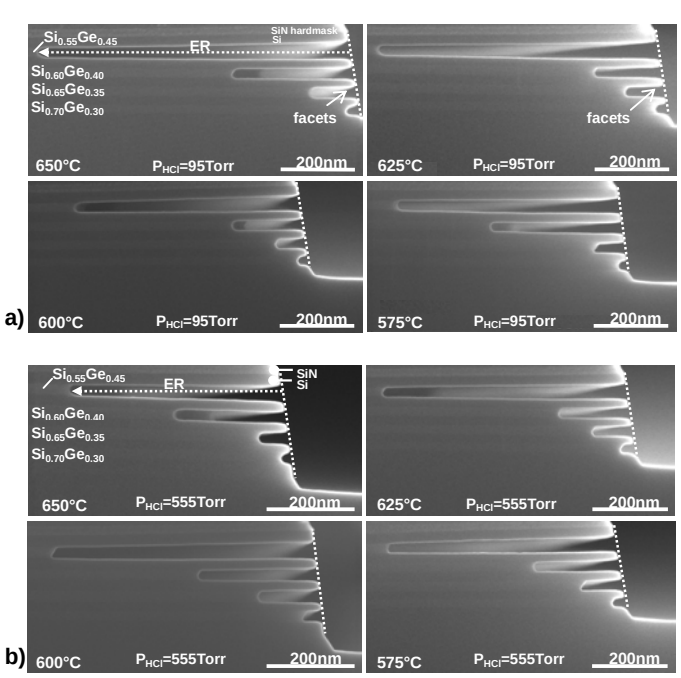

Figure 1 : SEM cross-section observations after lateral etch of $Si_{1-x}Ge_x$ layers between 575°C and 650°C with the HCl/H_2 gas mixture at P_{HCl}=95Torr (a) and P_{HCl}=555Torr (b). X is ranging from 0.30 (bottom layer) to 0.45 (top layer).

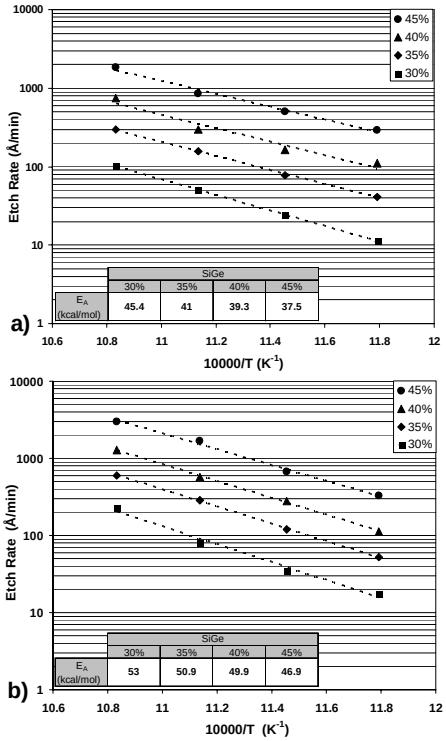

Figure 2: Arrhenius plots of the lateral etch kinetics of $Si_{1-x}Ge_x$ alloys with 0.30<x<0.45 between 575°C and 650°C at P_{HCl}=95Torr (a) and P_{HCl}=555Torr (b). The apparent activation energies are also reported in inserts.

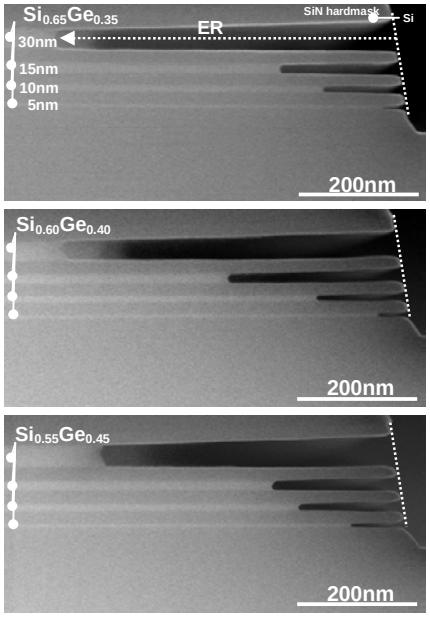

Figure 3 : SEM observations after lateral etch of $Si_{1-x}Ge_x$ layers with various thicknesses at 600°C and P_{HCl}=555Torr. SiGe thicknesses are ranging from 5nm (bottom layer) to 30nm (top layer).

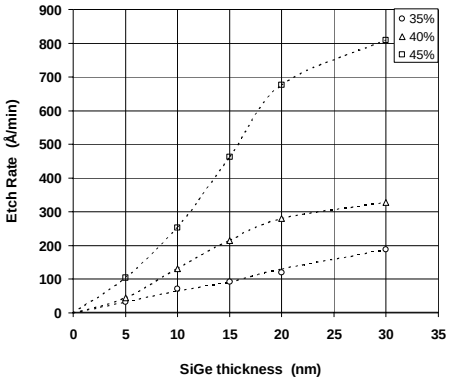

Figure 4 : Etch Rate variations as a function of the $Si_{1-x}Ge_x$ layers thicknesses for 0.35<x<0.45. HCl etch was performed at 600°C and 555Torr.

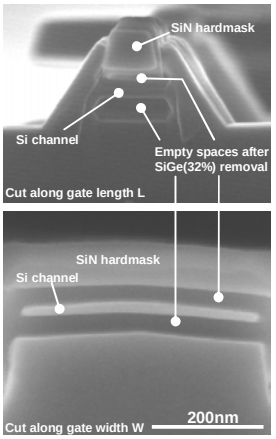

Figure 5: SEM cross-section along the gate length (top) and gate width (bottom) directions of the DG architecture.

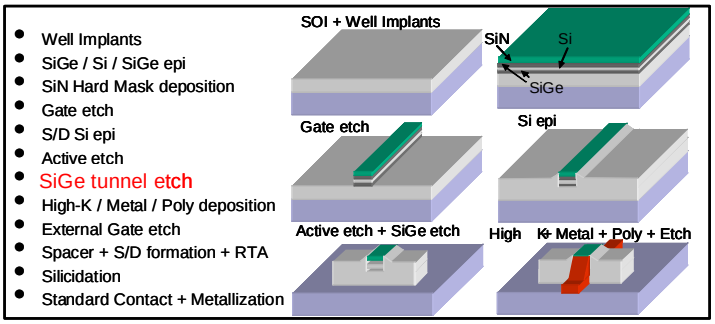

Figure 6: Description of the DG fabrication process

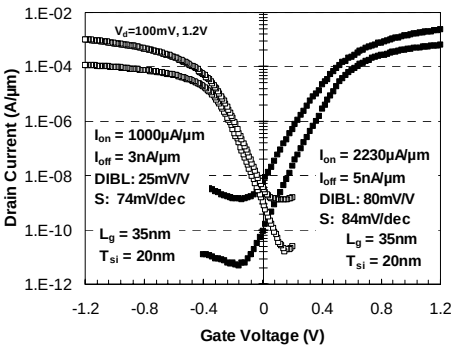

Figure 7: $I_d(V_g)$ characteristics of 35nm gate length double gate devices