A-6-1 Effects of O_2 Plasma Treatment on the Reliabilities of Metal Gate/High-k Dielectric MOSFETs

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1. Introduction

Metal gate/high-k dielectric stacks have decreased gate leakage due to their increased physical thickness for the same equivalent oxide thickness (EOT), which is extremely useful for low standby power applications [1-4]. During gate patterning, however, it has been reported that a dry etch or an HF-based wet etch led to process-induced damage (PID) and undercut of high-k dielectric at the gate edge region [5]. The recessed high-k structure shows significant high gate edge leakage current due to the leakage path formation in the heterogeneous interface between the high-k dielectric and the capping nitride layer [6].

To solve these problems, a recent approach has employed an in-situ O_2 plasma treatment for curing the PID [7]. Another study showed that low temperature plasma selective oxidation enhanced device characteristics of tungsten poly-metal gate transistors for memory applications [8]. However, the effects of the O_2 plasma treatment on the reliability of MOSFETs with high-k dielectric and metal gate have not been studied systematically. In this work, therefore, we investigated device characteristics and positive bias temperature instability (PBTI) and hot carrier injection (HCI) reliability for both of the O_2 and N_2 plasma-treated metal gate/high-k dielectric MOSFETs.

2. Experiments

The conventional high-k transistor process flow fabricated in this study is shown in Fig. 1. HfON films 2.5nm thick were deposited using atomic layer deposition (ALD) and followed by post-deposition annealing at 700°C in NH_3 ambient. Then, 10nm ALD TiN/100nm poly-Si gate stacks were deposited as an electrode, which was etched with a HBr- or Cl_2-based plasma process stopping on high-k. The remained high-k film in the source/drain (S/D) area was removed by low pressure, high density plasma using CO mixed with BCl_3. An in situ plasma treatment with O_2 or control N_2 was performed after the gate etch step (Fig. 1). A 5nm nitride was deposited on all samples before halo/extension formation to encapsulate the gate stacks.

3. Results and Discussion

Transistor current-voltage (I-V) characteristics for the HfON treated with O_2 or N_2 are shown in Fig. 2. The O_2 plasma-treated device exhibited a 20X lower off-state leakage current and slightly lower drain-induced barrier leakage (DIBL) with a reasonable I_{on} was achieved for compared to the N_2-treated sample. From the capacitance voltage (CV) curves of the perimeter-intensive array transistor (Fig. 3) and the gate-induced drain leakage (GIDL) characteristics (Fig. 4), the gate bird's beak and the gate overlap area seem to be similar for both plasma conditions. At a lower drain-to-gate voltage (V_{DG}) (V_g=0V), however, the N_2-treated sample showed larger drain current (I_d) than the O_2 plasma sample, which is attributed to the gate edge leakage [6, 7]. Therefore, the O_2 plasma treatment can be exploited for mitigating the leakage path formation in the heterogeneous interface between the high-k dielectric and the capping nitride layer. How this O_2 plasma treatment affects device reliability therefore needs to be studied.

Fig. 5 and 6 show the threshold voltage (V_{th}) shift induced by PBTI in HfON with either the O_2 or N_2 plasma treatment. Both the O_2- and N_2-treated devices showed similar V_{th} degradation and recovery behavior, indicating that neither post-gate etch treatment affected the dielectric characteristics. To investigate the gate edge effects, a hot carrier stress test was performed because accelerated carriers inject at the gate edge. From the results of hot carrier stress, we observed not only smaller V_{th} degradation but also a higher recovery rate with the O_2 plasma treatment (Fig. 7). The PBTI results suggest that the PBTI-induced V_{th} shift is attributed to transient charge trapping. Therefore, the trapped charges can be easily detrapped once a relaxation bias is applied. However, the injected hot carriers at the gate edge led to permanent damage in the dielectric, which was the reason for less V_{th} recovery during the relaxation stage. Furthermore, the heterogeneous leakage path in the gate edge region created deeper traps during HCI stress (Fig. 8). Consequently, the O_2-treated devices showed excellent device life time compared to that of the N_2-treated devices (Fig. 9).

During HCI stress, additionally, the drain edge of the high-k dielectric is affected by hot carriers and the cold carriers associated with PBTI also have an effect on the channel simultaneously [9]. Due to the transient charge trapping associated with PBTI, a high temperature HCI stress showed more significant initial V_{th} degradation compared to the HCI at room temperature (Fig. 10). In addition, the results from the high temperature HCI showed more significant drain current and transconductance (G_m) degradation in HfON with both the O_2 and N_2 treatment, indicating permanent damage generation (Fig. 11). From the results of the cyclic stress test, ΔV_{th} from the high temperature HCI was still higher than the other cases after the relaxation (Fig. 6, 7, and 12). Therefore, for short channel devices with metal gate/high-k dielectric, high temperature HCI degradation needs to be treated as a key reliability criterion but it is necessary to study its mechanism further. For high temperature HCI stress, the O_2 plasma-treated samples still showed better stress immunity (Fig. 12). The calculated device life time of the O_2 plasma-treated devices was also better (Fig. 13).

4. Conclusions

In this paper, the effects of an O_2 plasma treatment on CMOS devices with high-k dielectric were systematically investigated. Using the O_2 plasma treatment, we obtained a 20X lower off-state leakage current and enhanced stress immunity. In addition, high temperature HCI degradation was found to be a key reliability criterion for short channel metal gate/high-k dielectric devices.

Acknowledgements

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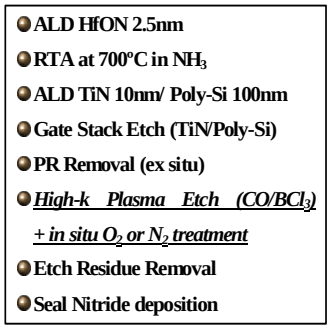
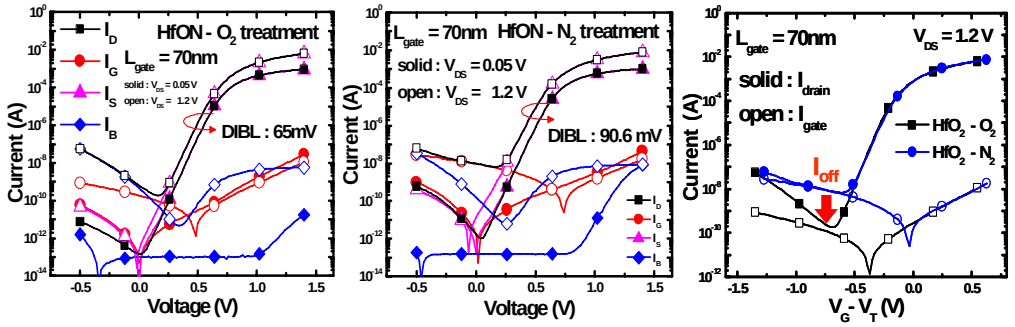


Fig 1. Gate stack process flow of MOSFET with TiN/HfON gate stack, high-k film is removed by plasma etch and treated with in suit O_2 or N_2 plasma



(a) (b) (c)

Fig 2. Transistor current-voltage (I-V) characteristics with (a) O_2 treatment and (b) N_2 treatment, and (c) normalized drain and gate current ; HfON O_2-treated samples show a 20X lower off-state leakage current and slightly lower DIBL compared to N_2 treated samples.

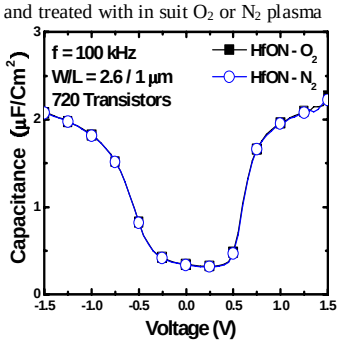


Fig 3. The CV curves of the perimeter -intensive array transistor in HfON with either an O_2 or N_2 plasma treatments ; The capacitance of both cases seems to be the same.

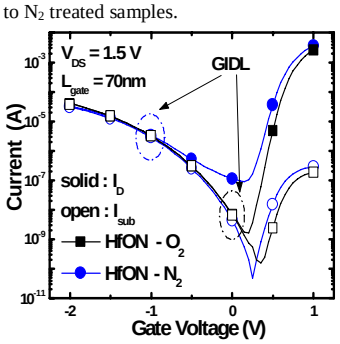


Fig 4. GIDL characteristics in HfON with O_2 or N_2 treatment; The GIDLs for both HfON devices show similar slopes. But, the GIDL-dominated point of the O_2-treate sample is lower than that of the N_2-treated sample

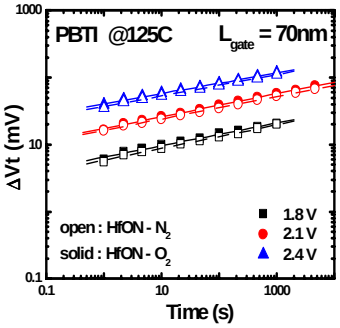


Fig 5. Comparison of V_{th} shifts induced by PBTI; PBTI of both O_2- and N_2-treated devices showed similar V_{th} degradation, indicating that PBTI is not correlated with the gate edge profile.

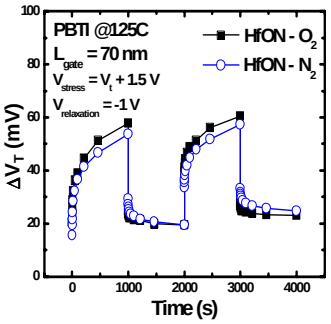


Fig 6. V_{th} recovery rate under V_{stress} = V_{th} +1.5V, and $V_{relaxation}$ = -1V; Similar recovery rate regardless of O_2 and N_2 treatment, indicating that PBTI is not correlated with the gate edge profile.

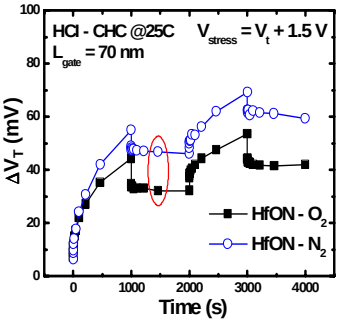


Fig. 7. Comparison of V_{th} shift induced by HCI; O_2 treated sample showed not only smaller V_{th} degradation and but also higher recovery rate compared to N_2 treated sample.

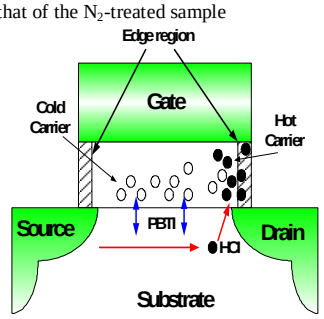


Fig 8. Schematic diagram of charge behavior during stress; Heterogeneous leakage path in the gate edge region creates deeper traps during HCI stress.

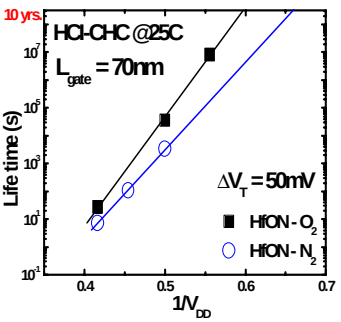


Fig 9. Comparison of HC lifetime between O_2 and N_2 plasma treated devices at 25°C. Excellent lifetime can be obtained by O_2 treated devices compared to N_2 treated devices.

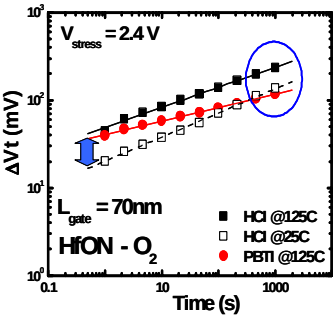


Fig 10. Comparison of V_{th} shift between HCI @25°C, HCI@125°C, and PBTI@ 125°C. For short channel devices, high temperature HCI degradation needs to be treated as a key reliability criterion.

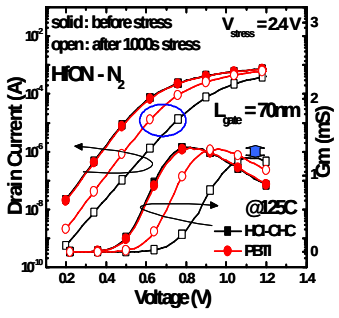


Fig 11. Comparison of drain current and G_m under V_{stress} = 2.4V after PBTI or HCI at 125°C; HCI characteristics showed more significant drain current and G_m degradation.

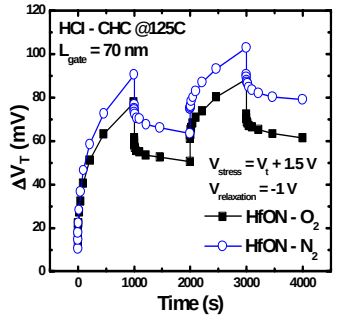


Fig 12. Comparison of V_{th} shift under V_{stress} = V_{th} +1.5V and $V_{relaxation}$ = -1V in HfON with O_2 or N_2 treatment; the O_2-treated sample showed less V_{th} degradation and a higher recovery rate.

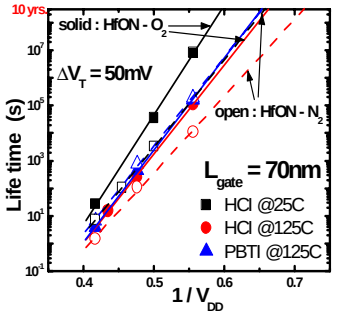


Fig 13. Lifetime comparison between HCI and PBTI, and O_2 and N_2 treatment. The devices with O_2 plasma treatment shows larger calculated device life time.

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