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The origin of slow and fast trapping under Bias Temperature Instability in HfSiO MOSFET

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1. Introduction

Hafnium based gate oxide is one of the most promising materials to implement next generation CMOS device. However, it has been suffered from reliability problem due to charge trapping in oxide layer [1]. Charge trapping in hafnium based gate oxide can be classified as slow and fast trapping due to fast transient charging effect [2]. The fast trapping cannot be sensed by a conventional DC BTI method because it happens less time than 1sec. To consider this fast trapping phenomena under BTI stress, "pulse on the fly"(P-OTF) method was introduced [3].

In order to improve film quality of hafnium based gate oxide, post deposition annealing (PDA) is essentially needed [4]. However, the analysis for PDA effect is not clear yet in a view of the origin of charge trapping under BTI stress. Therefore, in this work, we will investigate about the origin of slow and fast charge trapping in HfSiO transistors using a conventional DC and P-OTF BTI stress under different PDA conditions.

2. Experiment

After standard cleaning, 3nm-thick HfSiO was deposited by Atomic Layer Deposition (ALD) process. Three kinds of post deposition anneals (PDA) were performed in the NH_3 ambient (NH_3 PDA), in the NH_3 ambient followed by the oxygen ambient (NH_3+O_2 PDA), and in the NH_3 ambient followed by the enhanced oxygen ambient (NH_3+ehanced O_2 PDA). Additionally, densification annealing in the inert gas ambient was employed in all samples. After PDA, transistors under a conventional CMOS process were fabricated with poly silicon gate. Fig. 1 shows simple information of samples.

BTI characteristics were classified as slow and fast charge trapping as measurement method respectively. Conventional DC measurement was used to characterize a slow charge trapping and P-OTF method was implemented for fast charge trapping characteristics [5]. The measured area of all devices is 0.3um/10um (L/W).

3. Result and discussion

Figure 2 shows C-V characteristics as different PDA conditions. It was observed that the enhanced oxygen process increased in interfacial layer by excess oxygen sources.

Slow trapping characteristics

In order to estimate slow trapping characteristics in HfSiO, BTI using a conventional DC measurement was performed (figure 3 & 4). PBTI degradation is more severe than that of NBTI due to high concentration of trap sites existing in HfSiO near silicon conduction band. It is consistent with previously reported result [6]. As shown in figure 3, the V_{th} shift in nMOS reduced as re-oxidation order is increased. It has been reported that the main source of an electron trapping in hafnium based oxide relates to oxygen vacancies [7]. Therefore, the improvement of V_{th} shift by re-oxidation process can be explained as passivation of oxygen vacancies. In case of pMOS (figure 4), a weak PDA dependence was observed in NBTI characteristics. However, the V_{th} shift is reduced in the enhanced re-oxidation as same as nMOS behavior. Based on this result, it is speculated that the origin of slow trapping in pMOS also relates to oxygen vacancy.

To investigate contribution of interface traps in V_{th} shift, charge pumping measurement was performed. Figure 5 shows change rate of interface trap (N_{it}) as function of stress time. The interface traps in pMOS are more dominant comparing with those of nMOS. Small PDA dependence in N_{it} value was also observed. In other words, the increase in an interfacial layer is not dominant factor in V_{th} shift. In order to address the dominant layer causing V_{th} shift, oxide trap ($\Delta N_{ot}=C_{ox}\ \Delta V_{th}/q$) and ΔN_{it} value were compared as stress time (figure 6). Compared with oxide traps, in nMOS, the interface trap is negligible which means bulk traps in HfSiO layer are dominant source in V_{th} shift. However, in case of pMOS, the interface trap is one of dominant factors in V_{th} shift.

Fast trapping characteristics

Figure 7 and figure 8 show fast BTI characteristics by P-OTF measurement (t_m=100us). Similarly to DC results, fast traps in nMOS can be passivated by additional re-oxidation process. It was reported that oxygen vacancies existing in hafnium based oxide can be classified as two states which are a stable state and metastable state [3]. The oxygen vacancies of metastable state are main sources of fast trapping. Therefore, the reduction of oxygen vacancies by re-oxidation process can suppress fast trapping process. However, in contrast to nMOS, the degradation in pMOS under the enhanced re-oxidation condition is increased unlike DC results (figure 8). From this result, we can speculate that fast trapping source in pMOS is different with an oxygen vacancy.

To understand the origin of fast trapping source in pMOS more clearly, charge trapping and detrapping characteristics were evaluated. Figure 9 presents an initial amount of fast trapping after 3 sec stress. To consider pure fast trapping portion, the value by slow trapping (DC measurement) was subtracted. The enhanced re-oxidation PDA has the largest amount of fast trapping. Figure 10 shows detrapping characteristics. The inset of Fig. 10(a) explains measurement scheme of detrapping. After sufficient trapping stress (t_s), V_{th} was sensed in t_r(trapping sense) and t_f (detrapping sense) respectively. Same behavior as trapping characteristics is observed as shown in figure 10(c). Based on trapping and detrapping characteristics results, it is concluded that excess oxygen in HfSiO generates fast trapping sources in pMOS. According to the previous simulation report, hole conduction under NBTI relates to oxygen interstitial defect [7]. Therefore, it can be speculated that the increase in degradation by the enhanced re-oxidation process is caused by more generation of oxygen interstitial defects in HfSiO due to excess oxygen.

4. Conclusion

The origin of slow and fast trapping in HfSiO transistors was investigated with a conventional DC and P-OTF BTI stress under different PDA conditions. In case of nMOS, both slow and fast trapping are caused by oxygen vacancies in HfSiO layer. However, in pMOS, it is not only oxygen vacancies but also important interface traps in slow trapping. In addition, oxygen interstitial defects in HfSiO layer are an origin of fast trapping in HfSiO pMOS. Therefore, both oxygen vacancy and oxygen interstitial defects in HfSiO layer should be considered to implement a reliable CMOS device with HfSiO gate oxide.

Acknowledgement

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References

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	Gate Oxide	PDA Condition		Gate Metal
Sample 1	HfSiO	NH_3	RTA	Poly-Si
Sample 2		NH_3+O_2		
Sample 3		NH_3+ enhanced O_2		

Fig.1 Process information of samples. Three kinds of PDA conditions.

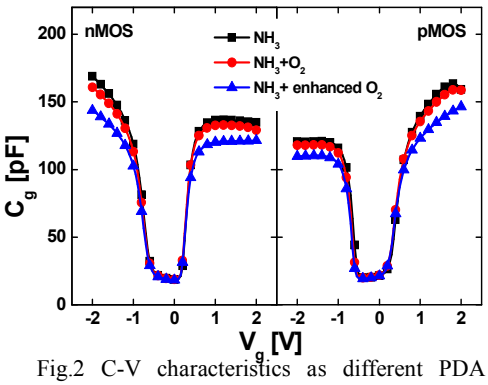

Fig.2 C-V characteristics as different PDA conditions.

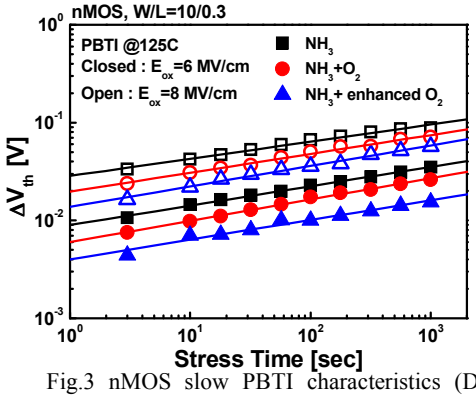

Fig.3 nMOS slow PBTI characteristics (DC measurement)

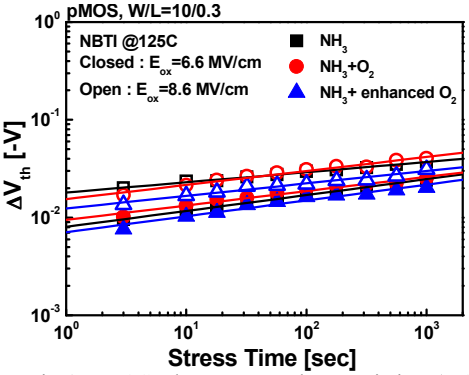

Fig.4 pMOS slow NBTI characteristics (DC measurement)

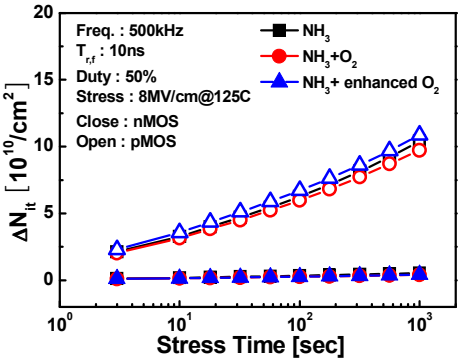

Fig.5 Change rate of interface state traps (ΔN_{it}) as function of stress time.

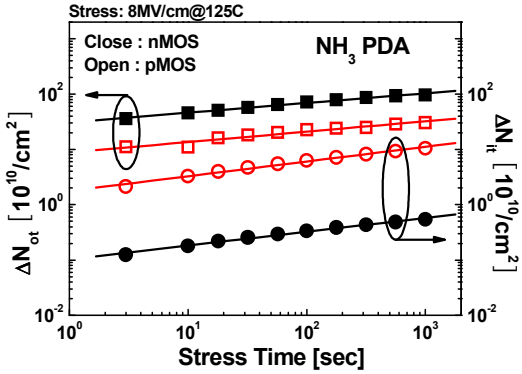

Fig.6 Comparison of oxide traps (N_{ot}) and interface state traps (N_{it}) from BTI results.

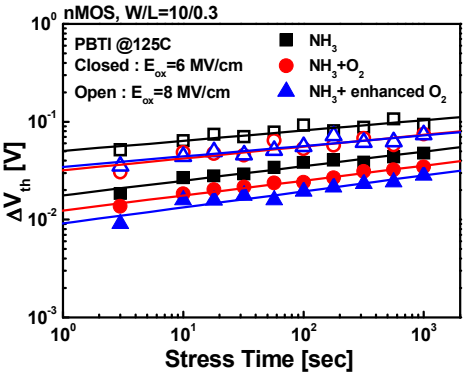

Fig.7 nMOS fast PBTI characteristics (P-OTF measurement, measurement time: t_m=100us)

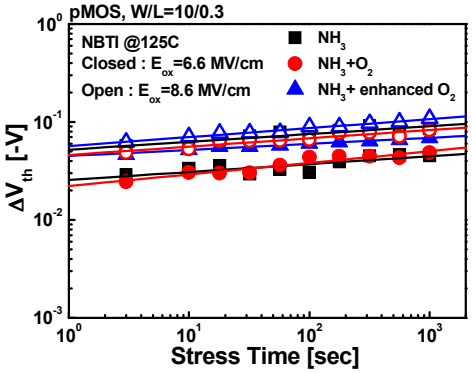

Fig.8 pMOS fast NBTI characteristics (P-OTF measurement, measurement time: t_m=100us)

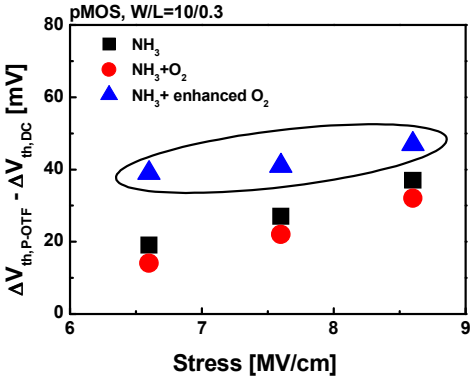

Fig.9 Initial amount of fast charge trapping after 3sec stress. ($\Delta V_{th,P\text{-}OTF}$-$\Delta V_{th,DC}$)

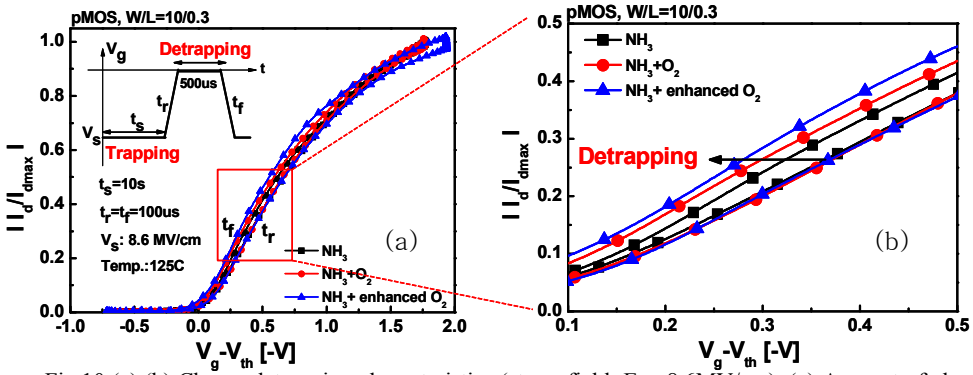

Fig.10 (a),(b) Charge detrapping characteristics (stress field: E_{ox}=8.6MV/cm). (c) Amount of charge detrapping as different stress field (detrapping $\Delta V_{th} = V_{th}(t_r) - V_{th}(t_f)$)