A-6-3

A Comparative Study of Plasma Source-Dependent Charging Polarity in MOSFETs with High-k and SiO_2 Gate Dielectrics

Koji Eriguchi[1], Masayuki Kamei[1], Daisuke Hamada[1], Kenji Okada[2] and Kouichi Ono[1]

[1]Graduate School of Engineering, Kyoto University
Yoshida-Honmachi, Sakyo-ku, Kyoto 606-8501, Japan
Phone: +81-75-753-5983 E-mail: eriguchi@kuaero.kyoto-u.ac.jp
[2]MIRAI-AIST, 16-1 Onogawa, Tsukuba, Ibaraki 305-8569, Japan

1. Introduction

From the viewpoints of reducing equivalent oxide thickness and controlling of gate leakage current, high-k dielectric materials are required to replace conventional SiO_2. Hafnium-based gate stack have been proposed to be the most promising candidate although reliability issues are being discussed [1],[2]. On the other hand, plasma-induced damage (PID) is a significant reliability issue for future devices, and PID to high-k gate dielectric has been recently reported by many groups [3]. However, there have been few comprehensive studies of PID to high-k devices under different plasma sources so far. In order to understand the mechanisms and the degradation of device performances during each manufacturing process step, the PID by various plasma sources should be investigated in detail.

The purpose of this paper is to evaluate the plasma-induced damage to MOS devices with high-k gate stack and those with SiO_2, by focusing on the impacts of plasma source type (Ar- and Cl-based gas mixture) and device charging polarities (n- or p-ch) on device degradations. Detail plasma diagnostics were also conducted in order to correlate plasma parameters to the changes in electrical characteristics as well as charging polarity. Plasma source-dependent charging polarity will be reported.

2. Experimental

N- and p-MOS devices were fabricated on p-type Si (100) substrate using a conventional CMOS process technology. High-k gate stack ($HfAlOx/SiO_2$) (denoted as "High-k") and thermally-grown SiO_2 with approximately similar physical thickness (~7 nm) are used as gate dielectric materials. Electrical thicknesses by capacitance-voltage (*C-V*) measurements are ~2.7 and ~7.4 nm for High-k and SiO_2, respectively. Al-interconnects was employed. Probing pads serve as antennas of "BOX" structures. Processed samples were mounted on wafer stage and exposed to Electron Cyclotron Resonance (ECR) plasma sources with power of 600 W, under the pressure of 1.0×10^{-2} Torr by two different Ar/O_2 and Cl/O_2 gas mixtures, denoted as "Ar" and "Cl", respectively. 13.56 MHz-RF bias with 200 W was supplied to wafer stage. Process durations (t_p) are 150 and 30 s for Ar and Cl, respectively. In order to determine the plasma parameters, the Langmuir probe and bias voltage measurements were carried out. Current-voltage (I_g-V_g, I_d-V_g) and *C-V* measurements were conducted for at least 12 difference devices to evaluate the deviation.

3. Results and Discussions

Plasma Diagnostics

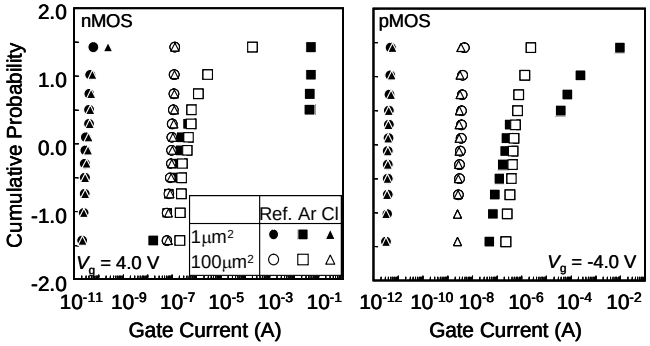
From the plasma diagnostics, the key parameters are determined as listed in Table I. Note that Ar-plasma is believed to be *electropositive*, and Cl-plasma, *electronegative*, and both types are widely used for fabrication processes.

Table I. Plasma parameters obtained from Langmuir probe and bias voltage measurements. u_B is Bohm velocity.

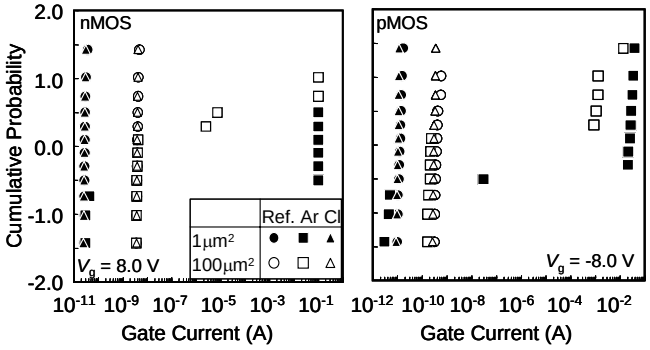
	V_{dc} (V)	n_e (10^{10}cm^{-3})	T_e (eV)	I_{ion} (mA)	u_B (cm^{-2}s^{-1})
"Ar"	-40	5.1	1.7	0.15	2.0×10^5
"Cl"	-50	1.2	16.5	11.7	6.3×10^5

Electrical Characterizations

Figures 1 show examples of gate leakage currents for various gate areas. Samples with smaller gate area correspond to larger antenna ratios. Severe charging is observed for Ar, and High-k devices are susceptible to charging damage. Figures 2 illustrate the flat band voltage shifts by



(a) High-k



(b) SiO_2

Fig. 1 Increases in I_g for damaged samples.

plasma exposures. MOS devices with High-k exhibits larger shifts compared to those with SiO_2. It should be noted that the shifts in nMOS with High-k are toward the "opposite" direction to those with SiO_2.

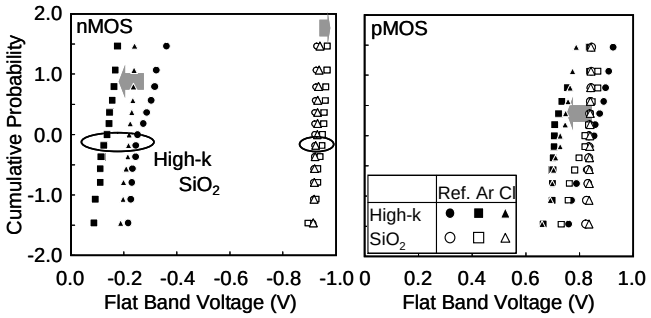
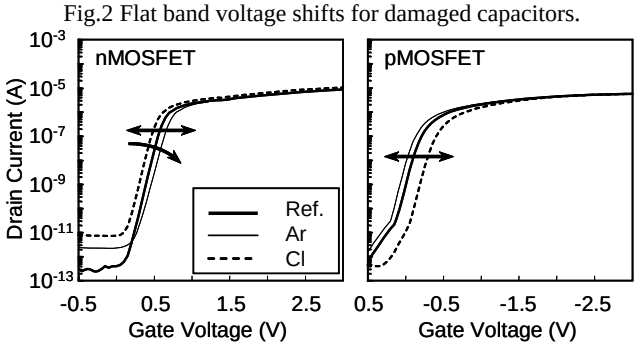
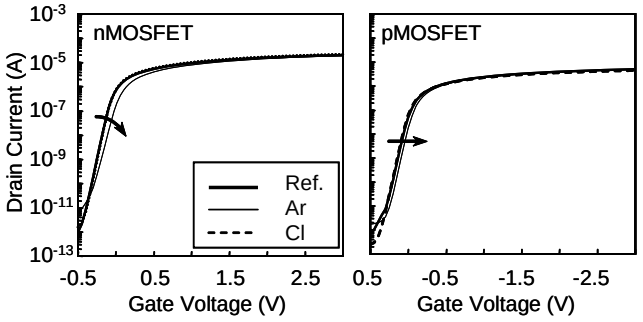


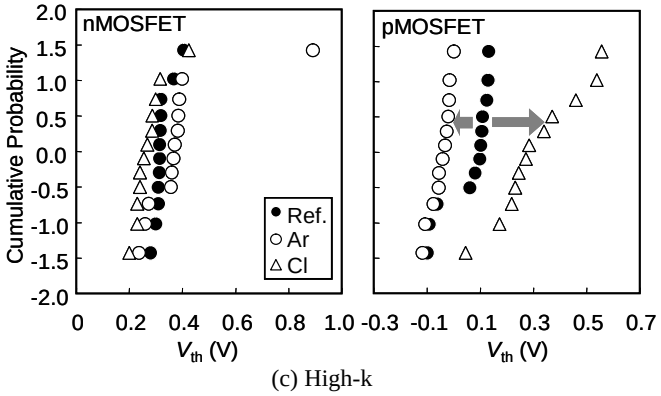
Fig.2 Flat band voltage shifts for damaged capacitors.



(a) High-k



(b) SiO_2



(c) High-k

Fig. 3 Characteristics of MOSFETs with High-k and SiO_2 exposed to Ar- and Cl-plasma sources. ($|V_{ds}|$=0.05 V).

Figures 3 (a) and (b) show typical examples of I_d-V_g for exposed samples and Fig.3 (c), the threshold voltage (V_{th}) shifts for High-k devices. The polarity of charging is the same for High-k and opposite for SiO_2 in terms of the threshold shifts. One should note that the direction of shifts in High-k depends on the plasma source type, Ar and Cl.

In the below are key experimental results in this study:

(1) High-k devices are more susceptible to charging damage, compared to SiO_2 devices.
(2) For pMOS with High-k, negative charge trapping ($-\Delta Q_{tr}$) is found for Ar, while positive charge trapping ($+\Delta Q_{tr}$) is observed in the lower damage case by Cl.
(3) For nMOS with High-k, both $-\Delta Q_{tr}$ and interface state generation (ΔN_{it}) are found for Ar, while $+\Delta Q_{tr}$ is observed in the lower damage case by Cl.
(4) For SiO_2 devices, ΔN_{it} in nMOS and $+\Delta Q_{tr}$ in pMOS are observed for Ar.

In the course of process time, a conduction current to the electrode is considered to consist of the nearly-constant ion current and the electron current with a "pulsed" form during a fraction of RF cycle [4]. This characteristic stress configuration provides complicated device degradation [5]. Based on the injected charge ($\sim I_{ion} \times t_p$) determined from Langmuir probing, the device surfaces are deduced to be more positively charged for Cl compared to Ar. Positive stress to the gate induces larger damage in pMOS even if source/drain plays a role as an alternative charging current path [6]. We do not have a positive explanation at present to "lower" charging mechanisms for Cl observed in Figs.1 and SiO_2 devices, as well as the characteristic charging polarity in I_d-V_g of High-k in Figs.3; we speculate that (1) the lower electron density/current, and/or (2) the etch reaction by Chlorine ions/radicals and the desorption of by-products with simultaneous electron attachment, might suppress (change) the charging damage (polarity) for Cl. Owing to the larger I_g (in the present thickness range [6]), intrinsic defective nature (larger defect generation probability), and an asymmetric energy band structure of high-k/interfacial SiO_2, High-k devices (in particular, pMOS) are more sensitive to stress configurations formed by plasma sources, compared to SiO_2, as seen in Figs.3 (a) and (c). The plasma source type and charging polarity should be considered for PID studies of High-k devices.

4. Conclusions

We found that high-k devices are more susceptible to plasma charging, compared to SiO_2 devices and that the charging polarity strongly depends on plasma sources. The observed plasma source-dependent charging polarity for high-k devices, in particular pMOS, should be involved in future plasma process designs and device design rules.

Acknowledgements

Acknowledgements are made to Dr. H. Ota at MIRAI-AIST, Dr. T. Nabatame at MIRAI-ASET, and Prof. A. Toriumi at University of Tokyo for their fruitful discussions. This work was partly supported by NEDO project.

References

[1] A. Kerber, et al., Int. Rel. Phys. Symp. Proc., 41 (2003).
[2] K. Okada, et al., Int. Rel. Phys. Symp. Proc., 36 (2007).
[3] C. D. Young, et al., Int. Rel. Phys. Symp. Proc., 67 (2007).
[4] K. P. Cheung, "*Plasma Charging Damage*", Springer, 2000.
[5] K. Eriguchi et al., in Proc. 6th Int. Conf. Reactive Plasmas and 23rd Symp. Plasma Processing, 5 (2006).
[6] M. Kamei, et al., to be presented at Int. Conf. IC Design and Technol. (2007).