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Suppression of Gate-Edge Metamorphoses of Metal/High-k Gate Stack by Low-Temperature, Cl-Free SiN Offset Spacer and its Impact on Scaled MOSFETs

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Abstract

Three SiN offset spacers were compared in terms of gate-edge metamorphoses (GEM) of a TaSiN/HfSiON gate stack. From the edge-emphasized C-V characteristics and $g_{m,max}^{-1}$-L_g plots, low-temperature, Cl-free SiN offset spacer was found to minimize the fixed charge in HfSiON on the gate edges and to keep the long-channel properties in the shortest channel. As a result, a significantly higher drive current was obtained with the low-temperature, Cl-free SiN offset spacer in short channel MOSFETs.

1. Introduction

Metal/high-k gate stack is required for aggressively scaled MOSFETs. Extensive investigations searching for a good metal/high-k have been done so far, but most of them focused on the bulk properties of the stacks. The edge properties, however, should be taken into account as well, first because the metal/high-k stack will be introduced in a device with a 20-nm long gate or a shorter one and secondly because metal/high-k stacks are less robust than poly-Si/SiON ones. As is illustrated in **Fig. 1**, the gate-edge metamorphoses (GEM) may appear in EOT increase [1, 2], shift in effective workfunction of the gate [3], or fixed charge in the high-k itself or its interfaces [4]. They will enhance a short channel effect (SCE) or reduce the drain current. Another GEM appears in a composition, typically N and O, of the metal or the high-k.

The offset spacer has a big impact on GEM because it directly contacts both the metal and the high-k during the high-temperature activation annealing. This is the reason why the offset spacers have been investigated in this study.

2. Experimental

Fig. 2 displays a STEM image of our typical gate stack. One of the three 10-nm thick films were deposited on a W/TaSiN/HfSiON gate stack as an offset spacer, that is, DCS-SiN (dichlorosilane-SiH_2Cl_2+NH_3, 760ºC), HCD-SiN (hexachlorodisilane-Si_2Cl_6+NH_3, 600ºC), and MS-SiN (monosilane-SiH_4+NH_3, 400ºC). The HCD- and DCS-SiN were deposited in a batch-type CVD apparatus while the MS-SiN was in a single-wafer "hot-wire" one. During the MS-SiN deposition, the wafer was kept at about 400ºC while the tungsten wires inside the reactor were at about 1800ºC. The MS-SiN is featured by its low process temperature at 400°C and Cl-free composition. Except for the offset spacers, the devices were fabricated in the same gate-first process with a spike annealing at 1000ºC (**Fig. 3**).

The three offset spacers were also applied to Poly-Si/HfSiON devices. In order to clearly investigate the effect of the offset spacers, these devices were intentionally fabricated without sidewall oxidation of the gate electrodes.

3. Results and Discussion

Fig. 4 shows the C-V characteristics for each SiN spacer. There is virtually no difference between the three curves for a square capacitor with 40 μm of the gate edge length (L_E) (**Fig. 4 (a)**). On the contrary, about 100 mV of positive shift is observed for the edge-emphasized DCS-SiN capacitor with L_E=4000 μm (**Fig. 4 (b)**). This shift clearly represents the GEM in TaSiN/HfSiON stack. The shift, however, is not observed for Poly-Si/HfSiON stack (**Fig. 4 (C)**).

The inverse of the maximum transconductance $g_{m,max}$ is plotted against L_g in **Fig. 5 (a)**. Each $g_{m,max}^{-1}$-L_g curve is characterized by three parameters; the slope ρ for large L_g, the y-intercept $g_{m,max,0}^{-1}$ extracted from a linear extrapolation with ρ at L_g=0 nm, and L_{GEM} with saturated $g_{m,max}$ even though L_g decreases. Since ρ represents the channel resistance, the parallel straight lines means the same long-channel properties. The offset $g_{m,max,0}^{-1}$ is the parasitic resistance that is attributed to the channel edges and the outside of the channel, such as S/D resistance and contact resistance. Since the three devices differs only in their spacers, the difference in $g_{m,max,0}$ reflects the channel-edge properties.

The smallest $g_{m,max,0}^{-1}$ and L_{GEM} is obtained by FET with MS-SiN (MS), so its drivability outstands especially in short-channel devices. Judging from the fact that MS curve is linearly extended to the smallest L_g, it is found that MS does not improve the short-channel properties, but that it just keeps the long-channel properties in a shorter one. This least damaging nature is estimated to be derived from the Cl-free composition and the low-temperature process [5].

Fig. 5 (b) shows the $g_{m,max}^{-1}$-L_g plots for Poly-Si/HfSiON. The difference is relatively small, but MS still had the largest $g_{m,max,0}$. By comparing **Fig. 5 (a) and (b)**, it is found that TaSiN/HfSiON is more fragile than Poly-Si/HfSiON. This corresponded to **Fig. 4 (b) and (c)**.

The roll-off characteristics are shown in **Fig. 6**. Although V_{th} for MS ($V_{th,MS}$) is smaller than $V_{th,HCD}$ at L_g<200 nm, MS does not suffer from a severer SCE. Shift in ϕ_m on the gate edges does not decrease $g_{m,max}$. EOT increase or D_{it} enhances SCE. So we speculate that the GEM or the parasitic resistance is mainly due to the fixed charge in high-k on the gate edges that simultaneously increases V_{th}, decreases $g_{m,max}$, and keeps the subthreshold swing comparable to the other.

Fig. 7 shows I_d-V_g curves for TaSiN/HfSiON. The difference is negligibly small for L_g=10 μm while that both in V_{th} and I_d is clearly observed for L_g=80 nm. This excellent short-channel drivability for MS is also proved by I_d-V_d curves in **Fig. 8**. **Fig. 9** shows I_{on}-I_{off} plots for the three offset spacers. Because of the excellent drivability in short channels, about 30 % gain of I_{on} at the same 10^{-9} A/μm of I_{off} is obtained by the MS.

4. Conclusion

Metal/high-k MOSFETs with a low-temperature, Cl-free SiN offset spacer is promising for its significantly higher drivability in short-channel devices by minimizing gate-edge metamorphoses.

References

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[2] T. Watanabe et al., IEDM Tech. Dig., p. 507, 2004.
[3] N. Mise et al., accepted in Microelectronic Engineering.
[4] Y. Yasuda et al., VLSI Tech. Dig., p. 131, 2006.
[5] S. Sakashita et al., SSDM, p. 854, 2005.

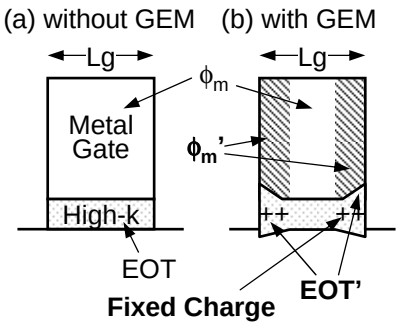


Fig. 1 Gate stack properties without (a) and with GEM (b).

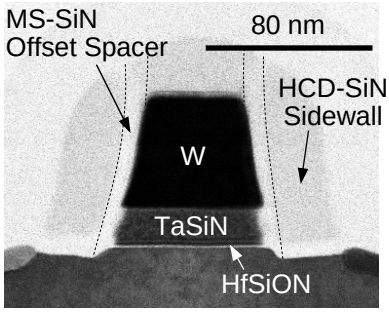


Fig. 2 STEM image of 10-nm thick MS-SiN offset spacer applied to TaSiN/HfSiON gate stack.

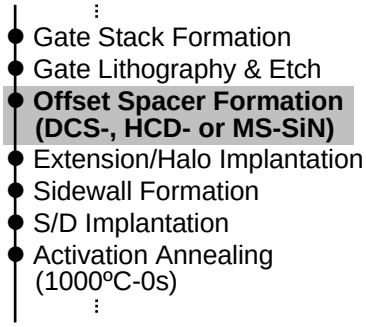


Fig. 3 Main process steps.

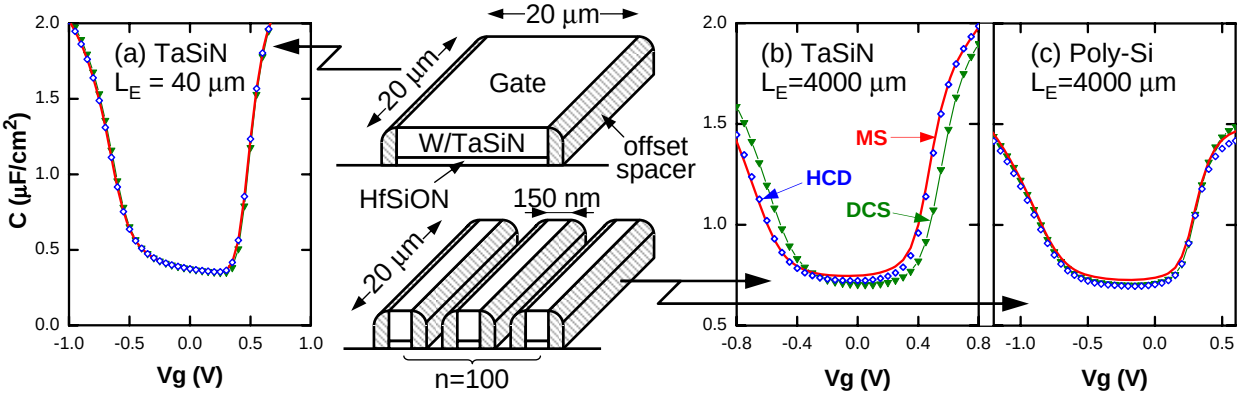
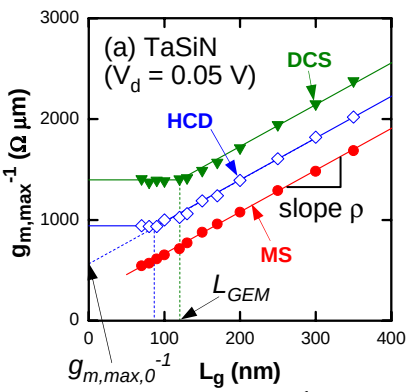


Fig. 4 CV-curves for square capacitors (a) and edge-emphasized capacitors with comb pattern (b).



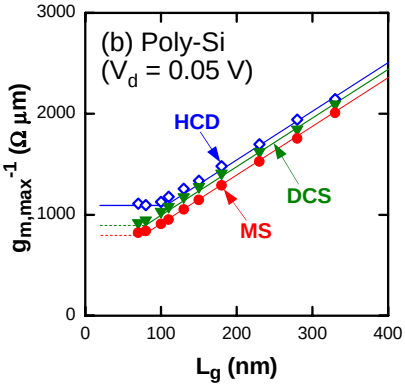


Fig. 5 $g_{m,max}^{-1}$–L_g plots for three offset spacers with TaSiN gate (a) and Poly-Si gate (b).

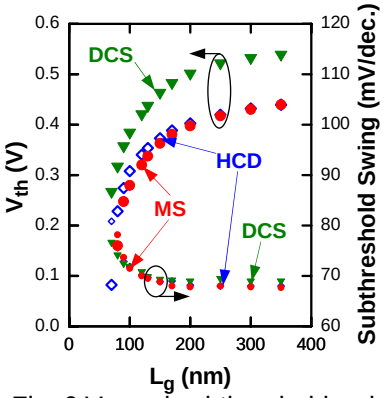


Fig. 6 V_{th} and subthreshold swing as a function of L_g.

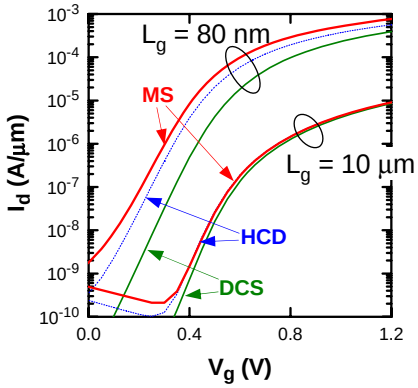


Fig. 7 I_d-V_g curves at V_d = 1.1 V.

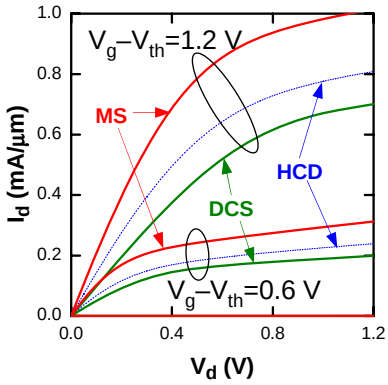


Fig. 8 I_d-V_d curves for L_g=80 nm.

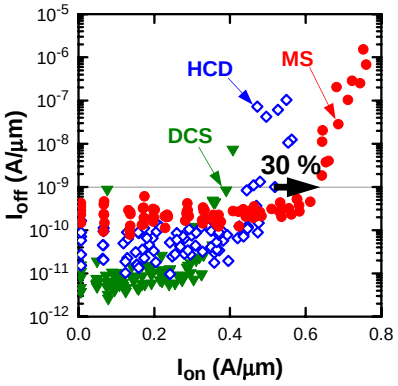


Fig. 9 I_{on}-I_{off} plots.