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Anomalous positive V_{fb} shift in $HfAlO_x$ MOS gate stacks

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1. Introduction

Aggressive scaling of MOSFETs for performance improvement causes a number of challenging problems such as high gate leakage current and poly-Si gate depletion. To overcome these issues, alternative high-k dielectrics such as HfO_2 and metal gate electrodes with band-edge work function are required. In addition, Al_2O_3 capped HfO_2 and $HfAlO_x$ dielectrics have also been studied as one of the technologies for tuning the V_{th} of pMOSFET [1,2].

Furthermore, the problem of V_{fb} "roll-off" phenomena have been reported in metal/Hf-based high-k stacks [3,4] in addition to the Fermi-level pinning. It makes V_{fb} tuning intrinsically difficult even by choosing metal gate electrode. This paper further reports an interesting behavior of anomalous V_{fb} shift towards the positive voltage for Al-based high-k MOS stacks for the first time, which we refer to as "V_{fb} roll-up". Apparently, this effect should be taken into account to adjust V_{fb} in addition to the Fermi-level pinning at the top interface of high-k and the V_{fb} roll-off at the bottom interface [5]. Thus, it is of a great importance to understand and control the V_{fb} roll-off/up behaviors for metal/Al-incorporated dielectrics gate stack application. In this work, we mainly focus on the implication of the V_{fb} roll-up behavior in $HfAlO_x$ dielectrics.

2. Experimental

MOS capacitors were fabricated on p-type Si wafers with SiO_2 interlayer and $HfAlO_x$ dielectrics. 20 nm-thick SiO_2 films grown by thermal oxidization were firstly wet etched to a terraced structure with thicknesses ranging from 0 to 17 nm. After thermal re-oxidization at 1000 ^oC, 3 nm-thick $Hf_{1-y}Al_yO_x$ (y=0~1) layer was deposited on the terraced-SiO_2 by MOCVD. Post deposition annealing (PDA) was performed at 800 ^oC for 1 s in O_2. NiSi/TiN/W was used as a gate electrode. Post Si deposition annealing (PSA) [6] process was performed at 1000 ^oC in N_2. To study the mechanism of the V_{fb} roll-up, a W (30 nm)/Al_2O_3/Terraced-SiO_2 structure was also prepared with PDA at 1000 ^oC. All the samples were subjected to H_2 annealing at 400 ^oC for 30 min.

3. Results and discussion

Figure 1 shows the typical V_{fb}-EOT plots for NiSi/TiN/W/$Hf_{1-y}Al_yO_x$/Terraced-SiO_2/Si MOS capacitors. Equivalent oxide thickness (EOT) and V_{fb} were extracted from the fitted ideal C-V curves. It was observed that an anomalous V_{fb} shift towards positive voltage occurs in $Hf_{1-y}Al_yO_x$ and Al_2O_3 dielectrics as the EOT was scaled to below ~6-7 nm, i.e., V_{fb} roll-up effect. The magnitude of V_{fb} roll-up increases with an increase of Al content of $Hf_{1-y}Al_yO_x$ dielectrics. The V_{fb} roll-off observed in Fig.1 will not be discussed in this paper, while we focus on the roll-up behavior.

A typical V_{fb}-EOT plot and D_{it}, and the corresponding C-V curves for NiSi/TiN/W/Al_2O_3/terraced-SiO_2/Si MOS capacitors are shown in **Figs. 2 and 3**. Well-behaved C-V characteristics are observed both in the roll-up and normal EOT regions. In addition, nearly negligible hysteresis in C-V curves and $(5\text{-}7)\times10^{11}$ $eV^{-1}cm^{-2}$ of D_{it} at Si midgap are also obtained for these two EOT regions, indicating very little difference in dielectric film properties.

Next, an effect of thermal budget, which is essentially important for V_{fb} roll-off [4], on the V_{fb} roll-up was examined for W/Al_2O_3/Terraced-SiO_2/Si structure. In this case, after Al_2O_3 deposition at 500 ºC, only PDA was performed at 1000 ºC. PDA time was varied in the range of 1-100 s with 100 Pa O_2. The PDA time dependence of V_{fb}-EOT is shown in **Fig. 4**. It is evident that the thermal budget has a significant effect on the variation of V_{fb}. Compared to the sample with SiO_2 dielectric, all of the V_{fb}-EOT plots for the Al_2O_3 gate stacks shift towards the positive voltage, and as the EOT is scaled down to below ~6-7 nm, anomalous V_{fb} roll-up occurs. It is noteworthy that for the samples with Al_2O_3 layer, even in the case of no PDA, the V_{fb}-EOT plot was also as a whole shifted positively with respect to the SiO_2 case. This could be attributed to a dipole layer lying at the Al_2O_3/SiO_2 interface [7].

Figure 5(a) summarizes the PDA time dependences of V_{fb} roll-up magnitude (ΔV_{fb}) and onset EOT of roll-up ($EOT_{roll\text{-}up}$). As schematically depicted in **Fig. 5(b)**, the difference in the actual V_{fb} and the expected V_{fb} is defined as ΔV_{fb}, while the $EOT_{roll\text{-}up}$ is referred to the starting point of V_{fb} roll-up. Both the values of ΔV_{fb} and $EOT_{roll\text{-}up}$ increase linearly as a function of the square root of PDA time ($t^{1/2}$), in other words, longer PDA time enlarges the roll-up magnitude and makes the roll-up behavior to occur even at thicker SiO_2 region. If from the viewpoint of charge, the ΔV_{fb} and $EOT_{roll\text{-}up}$ are affected by charge variation in dielectrics, longer PDA time may promote the charge generation both in amount and in regime in dielectrics. Therefore, the possible charge variation may be correlated with atom diffusion in dielectrics, and dominate the V_{fb} roll-up behavior.

To obtain an evidence of the diffusion process thermally activated in the PDA, a back-side SIMS analysis was performed on the samples with structure of W/Al_2O_3 (3 nm)/SiO_2 (20 nm)/Si. PDA processes were carried out at 1000^o C for 10 s and 100 s, respectively, followed by W gate deposition. Prior to back-side SIMS analysis, the Si wafer side was chemically etched down to the SiO_2 interfacial layer for precisely determining the possible interdiffusion of various species. Back-side SIMS depth profiles evaluated for samples with and without 1000 ^oC PDA are compared in **Fig. 6**. Al diffusion from Al_2O_3 layer into SiO_2 interlayer was clearly observed. The longer PDA time causes the deeper diffusion of Al into SiO_2 interlayer.

The results of **Fig. 5** and **6** show that Al diffusion seems to play an important role in the anomalous V_{fb} variation. Although we cannot uniquely assign the cause of V_{fb} roll-up to the Al diffusion, the clear PDA time dependence of Al profile in SiO_2 implies a possible role of Al diffusion for the anomalous V_{fb} change. It is likely that the Al diffusion-induced defects or charges are generated in Al_2O_3, SiO_2 and presumably in Si substrate. Furthermore, with the significant decrease in SiO_2

interlayer thickness, the induced charges in the dielectrics layer appear to cause the V_{fb} roll-up behavior.

3. Conclusions

It is pointed out for the first time that anomalous V_{fb} shift towards the positive voltage (V_{fb} roll-up) appears in Al-incorporated high-k gate stacks with decreasing SiO_2 interlayer thickness. Al diffusion–induced charged sites both in high-k layer and in SiO_2 interlayer are attributed to the V_{fb} roll-up effect. This should be taken into consideration for quantitatively adjusting V_{fb} and could be used for further tuning V_{fb} in pMOS devices.

Acknowledgements

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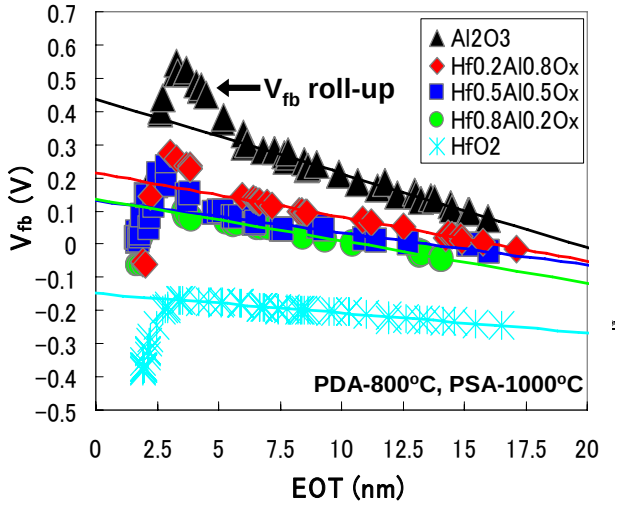

Fig. 1. Dependence of V_{fb} on EOT for the samples with NiSi/TiN/W/$HfAlO_x$/Terraced-SiO_2/Si structure. An anomalous V_{fb} shift towards positive voltage occurs as the EOT was scaled to below ~6-7 nm in $HfAlO_x$ and Al_2O_3.

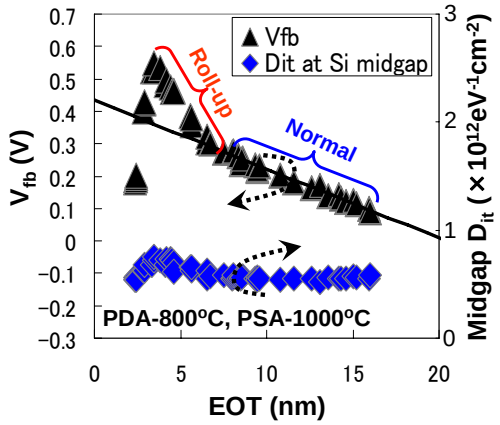

Fig. 2. A typical V_{fb}-EOT plot for the sample with a structure of NiSi/TiN/WAl_2O_3/Terraced-SiO_2/Si. Comparable D_{it} at Si midgap (~5-7×10^{11} $eV^{-1}cm^{-2}$) was obtained for the roll-up and normal EOT regions.

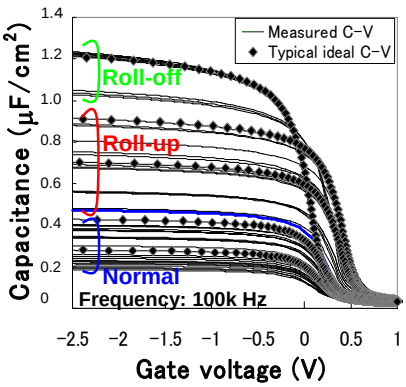

Fig. 3. C-V curves for the NiSi/TiN/W/Al_2O_3/Terraced-SiO_2/Si sample. Well behaved C-V characteristics both in the roll-up and normal EOT regions indicate very little difference in dielectric film properties.

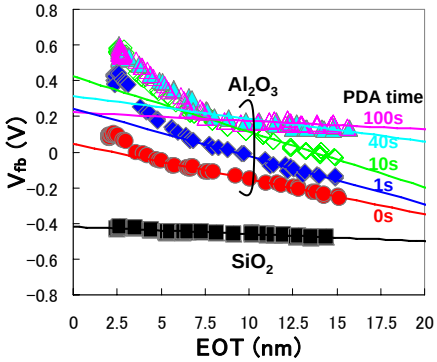

Fig. 4. PDA time dependence of V_{fb} vs EOT plots for the W/Al_2O_3/ Terraced-SiO_2/Si samples. Thermal budgets have a significant effect on the variation of V_{fb}.

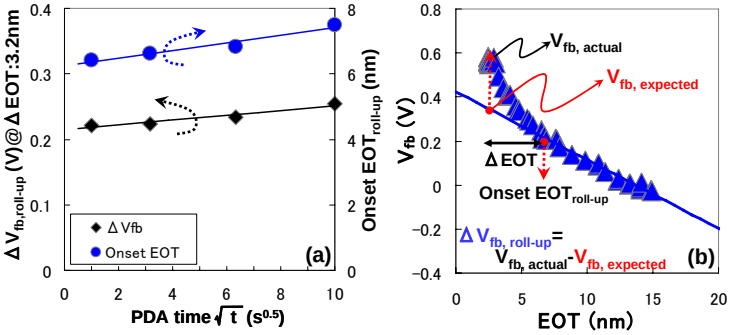

Fig. 5. PDA time dependences of ΔV_{fb} and onset $EOT_{roll\text{-}up}$ for the W/Al_2O_3/Terraced-SiO_2/Si samples (a), Definitions of ΔV_{fb} and $EOT_{roll\text{-}up}$ (ΔEOT) are given in (b).

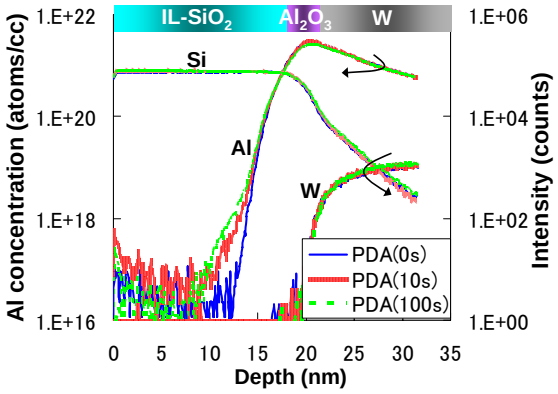

Fig. 6. Back-side SIMS depth profiles for the W/Al_2O_3/SiO_2 samples with and without 1000 ºC PDA. Al diffusion from Al_2O_3 layer into SiO_2 interlayer was clearly observed. The longer PDA time causes the deeper diffusion of Al into SiO_2 interlayer.