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Systematic studies on Fermi level pining of Hf-based high-k gate stacks

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1. Introduction

Metal/Hf-based high-*k* gate stacks have been expected as the alternative gate dielectric materials to ordinary SiO_2 in future LSIs [1], and they are planning to be used in the next generation LSIs by Intel and IBM. However, it is well-known that Hf-based high-k dielectrics reveal Fermi level pinning (FLP) [2-6], and effective work functions (WF) of p-like gate metals are almost independent of metal species [5,6]. It makes difficult to construct CMOS by gate-first processes. As for pining mechanism, it has been reported that interface reactions between HfO_2 and Si that generate O vacancies are responsible for FLP [2,3,6]. To avoid or to recover FLP, O injection to Hf-based gate stacks that aims to eliminate O vacancies, have been thought as an effective recipe [4,7,8]. In this paper, we theoretically show that O injection essentially leads to the interfacial SiO_2 growth under thermal equilibrium condition. Thus, FLP recovery by O injection is not hopeless to obtain very thin EOT that is required future Si devices. Moreover, we also discuss the mechanism of the forming gas anneal induced FLP and briefly comment on the recipe for obtaining band-edge-work-function metals.

2. Basic Concept of O Vacancy Model

Our O vacancy model [2,3,6] is that the final FLP position is governed by the enegetics of the reaction at HfO_2/Si interfaces. As illustrated in Fig. 1, when the Fermi level of a gate is pinned at the FLP position, O vacancy formation and O vacancy annihilation are balanced. This situation can be written by the following reaction equation.

$$\tfrac{1}{2}Si + (HfO_2) \leftrightarrow \tfrac{1}{2}SiO_2 + (HfO_2 + Vo^{2+} + 2e) \qquad (1)$$

FLP position is uniquely determined by the energetics of HfO_2/Si interface reaction, since energy gain by the electron transfer depend on the gate Fermi level as shown in Fig. 1.

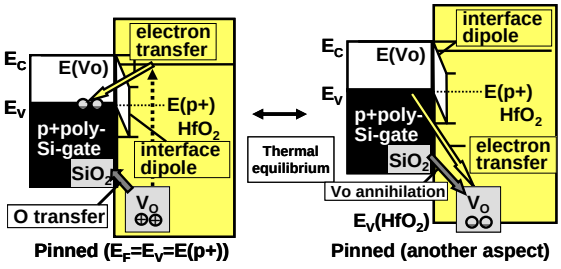

Fig.1: Schematic illustration of Fermi level pinning situation. As an example, the situation of the p+poly-Si pinning is shown. O vacancy generation and annihilation are balanced when the Fermi level pinning occurs.

In case of metal gate pinning, Vo generation occurs near the Si substrate and electrons transfer to gate metals. If generated O vacancies remain the same position near the substrate, electric field is formed inside the high-k film (Fig. 2 (a)). Thus, during high temperature process, they should move toward gate metals, resulting in no electric field formation inside the high-k film (Fig. 2 (b)). Moreover, this O vacancy distribution is energetically much more favorable than the initial O vacancy distribution.

3. Results and Discussions

3.1 O injection effect to aim FLP recovery

First, we discuss the O injection effect to aim FLP recovery. To recover FLP, elimination of O vacancies is crucial. In the pinning situation, Eq. (1) is satisfied. By using chemical potential, Eq. (1) can be written as follows.

$$\tfrac{1}{2}\mu(Si) = \tfrac{1}{2}\mu(SiO_2) + \mu(Vo^{2+}) + 2\mu(e) \qquad (2)$$

O vacancy elimination reaction can be written as follows.

$$(Vo^{2+} + 2e) + O \rightarrow (HfO_2 \text{ crystal}) \qquad (3)$$

By using chemical potential, Eq. (3) is expressed as

$$(\mu(Vo^{2+}) + 2\mu(e)) + \mu(O) > 0 \qquad (4)$$

In other words, O vacancy elimination should be exothermic. By combining Eq. (2) and (4), we can obtain the following relation.

$$\tfrac{1}{2}\mu(Si) + \mu(O) > \tfrac{1}{2}\mu(SiO_2) \qquad (5)$$

This equation means that the condition of O vacancy elimination is equivalent to the condition of SiO_2 interface

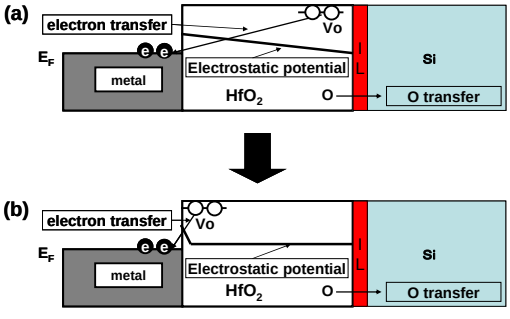

Fig.2: Initial (a) and final (b) O vacancy distributions. O vacancies move toward gate metals to stabilize the system.

layer growth by oxidizing a Si substrate. Eq. (5) also implies that Si substrate should be oxidized, if injected O can eliminate O vacancies. This clearly shows that FLP recovery due to O vacancy elimination by O injection and SiO_2 interface layer growth are essentially traded off when the system is under thermal equilibrium. Since recent SiO_2 interface layer thickness is quite thin (~0.7nm), O can easily penetrate into a Si substrate through a SiO_2 interface layer. Actually, recent RBS experiments show that O diffusion length in SiO_2 interface layer is about 2nm at 900C oxidation [9].

Schematic illustration of the above situation is shown in Fig. 3. As shown in this figure, there are no process windows that enable the recovery of effective WF of gate metals without SiO_2 interface layer growth in thermal equilibrium conditions.

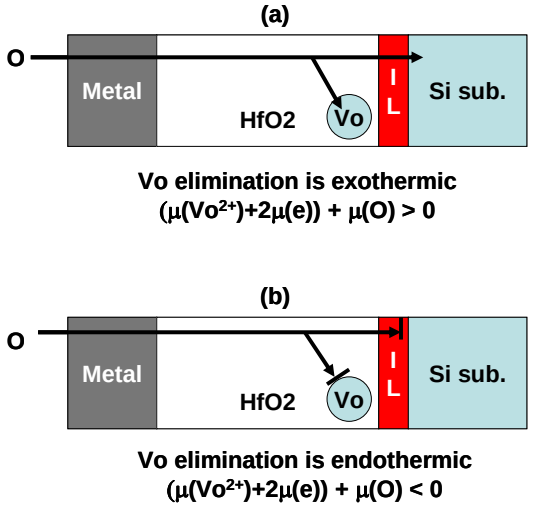

Fig.3: Schematic illustration of O injection effect to aim the elimination of O vacancies. (a) When O vacancy elimination is exothermic, both Vo elimination and Si substrate oxidation occur. As a result, undesirable EOT increase is unavoidable, although effective WF recovery is expected. (b) When O vacancy elimination is endothermic, neither Vo elimination nor Si substrate oxidation occurs. Although undesirable EOT increase does not occur, Fermi level pinning cannot be improved.

3.2 Effect of forming gas anneal

In this subsection, we consider the forming gas anneal effects. Forming gas anneal can form O vacancies in HfO_2 by reducing reaction ($O + H_2 \rightarrow H_2O$). Recent experiments show that energy gain from electron transfer from Vo to gate metals are very important for O vacancy generation by forming gas anneal [10]. In principle, O vacancy generation by forming gas anneal is exothermic. Thus, effective WFs of gate metals can decrease toward the conduction band of Si. However, after forming gas anneal, it is also reported that obtained effective WFs are almost independent of metal species (Fermi level pinning). These phenomena can also be explained naturally by our O vacancy model. In principle, metal effective WFs can become smaller when chemical potential of O in gate metal is small enough.

However, the existence of SiO_2 interface layer prevents decrease in effective WFs of gate metals. As shown in Fig. 1, the position of FLP corresponds to the effective WF of a gate metal at which O vacancy generation and O vacancy annihilation are balanced. In other words, O vacancy annihilation by reducing a SiO_2 interface layer naturally occurs when the metal effective WF is too small (Fig. 4). As a result, effective WFs of metals are also pinned near the pinning position of p+poly-Si gates after forming gas anneal. This is the reason why effective WFs of gate metals have also small dependence on metal species after forming gas annealing.

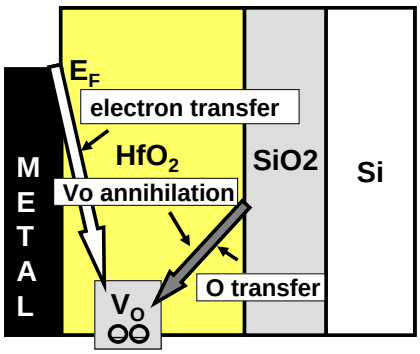

Fig.4: Schematic view of the mechanism of H_2 anneal induced Fermi level pinning. Higher Fermi level due to the generation of Vo makes Vo annihilation reaction by reducing a SiO_2 interface layer exothermic. As a result, Fermi level is pinned near the pining position of p+poly-Si gates.

3.3 Recipe for obtaining band-edge-work-function metals

As discussed in this paper, FLP cannot be avoided if the system reaches thermal equilibrium. To obtain band-edge metals, there are some possibilities. One is low temperature process which inhibits the system to reach thermal equilibrium. Another possibility is to change the energetics of interface reactions. For example, the use of Ge substrate seems promising. Since energy gain of GeO_2 formation is much smaller than that of SiO_2 formation, O transfer from HfO_2 to a Ge substrate becomes difficult.

4. Conclusion

We have systematically studied Fermi level pinning of Hf-based high-k gate stacks based on our O vacancy model. Our study shows that FLP cannot be avoided when the system is under thermal equilibrium. O injection to aim O vacancy elimination is hopeless, since O vacancy elimination condition is equivalent to the Si substrate oxidation which leads to the increase in EOT. We also studied the mechanism of FLP induced by forming gas anneal. FLP by forming gas anneal is governed by the O vacancy annihilation reaction by reducing SiO_2 interface layer. Moreover, we briefly discuss the recipe for obtaining band-edge-work-function metals.

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References

[1] G. D. Wilk et al., J. Appl. Phys. **89**, p.5243 (2001).
[2] K. Shiraishi et al., Tech. Dig. VLSI Tech. 2004 p.108 .
[3] K. Shiraishi et al., Jpn. J. Appl. Phys., 43, L1413 (2004).
[4] E. Cartier et al., Tech. Dig. VLSI Tech. 2005 p.230.
[5] B. H. Lee et al., materials today, **9**, 36 (2006).
[6] Y. Akasaka et al., Jpn. J. Appl. Phys., **45**, L1289 (2006)
[7] K. Ohmori et al., J. Appl. Phys. **101,** 084118 (2007).
[8] Y. Tsuchiya et al., Extend abstract of SSDM 2006 p.1132.
[9] Z. Ming et al., Appl. Phys. Lett., **88,** 153516 (2007).
[10] Y. Kita et al., 2007 Spring Meeting of Material Research. Society, San Francisco, USA, April 2007 H4.9.