

## Production-Worthy HfSiON Gate Dielectric Fabrication Enabling EOT Scalability Down to 0.86 nm and Excellent Reliability by Polyatomic Layer Chemical Vapor Deposition Technique

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### 1. Introduction

Among the high-*k* materials under investigation, Hf-silicates have emerged as the most promising candidates [1]. For fabrication of Hf-silicate films, Atomic Layer Deposition (ALD) technique [2] has been applied so far, but it has been difficult to achieve acceptable throughput for production. To fabricate high-quality film with sufficient throughput, we have developed the Polyatomic Layer Chemical Vapor Deposition (PLCVD) process in which ultra-thin film deposition and post-deposition O<sub>3</sub> treatment steps are repeated. Key concepts are film deposition in CVD mode to increase the growth rate and post-deposition treatment to the ultra-thin films to improve film quality [3]. In this paper, we report on excellent productivity of the PLCVD process and demonstration of EOT scalability (0.86 nm), high mobility (80% of SiO<sub>2</sub>) and high BTI reliability.

### 2. Experiment

The PLCVD Hf-silicate films were formed using a single-wafer reactor designed for 300-mm wafer processing using tetrakis (1-methoxy-2-methyl-2-propoxy)-hafnium (Hf[OC-(CH<sub>3</sub>)<sub>2</sub>CH<sub>2</sub>OCH<sub>3</sub>]<sub>4</sub>) and tetrakis(1-methoxy-2-methyl-2-propoxy)-silicon (Si[OC(CH<sub>3</sub>)<sub>2</sub>CH<sub>2</sub>OCH<sub>3</sub>]<sub>4</sub>) as the Hf and Si precursors, respectively. The schematic of PLCVD reaction is shown in Figure 1. First, the Hf and Si precursors were introduced into the reactor at around 400°C to deposit several layers of Hf-silicate film by self decomposition. Then after purging with N<sub>2</sub>, diluted O<sub>3</sub> was introduced into the reactor for 2-10 s to eliminate impurities. These process steps were repeated until the target thickness was formed. The process cycle time for a typical condition was around 1 min. We investigated two different process sequences: Hf and Si precursors were either introduced in the same step (co-injection, Fig.2 (a)) or in separate steps (lamine, Fig.2 (b)). For the electrical characterization of the films, MISFET samples were fabricated by forming Hf-silicate films of around 2-nm in thickness on 0.6-nm-thick SiON interfacial layers, followed by plasma nitridation and post-nitridation annealing at a temperature of 1000°C. Poly-silicon or TaSiN were used as the gate electrodes.

### 3. Results and Discussion

The average thicknesses and thickness uniformities of Hf-silicate films are shown in Figure 3 as a function of the number of process cycles. The film thicknesses increase at a rate of 0.5 nm/cycle, which is higher than the typical growth rate for the ALD process, 0.1nm/cycle [2]. Therefore, five times higher throughput than that for the ALD process can be achieved by the PLCVD process. Compared to the co-injection sequence, the lamine sequence is inferior in throughput by around 30%, due to the extra purge step. Good thickness uniformity of around 3% over a 300-mm wafer is also noted. Figure 4 shows the controllability of the Hf concentration in the HfSiO films. By changing the flow ratio (co-injection) or the injection time (lamine) of the Hf and Si sources, the Hf concentration can be varied from 30 to 100%. Figure 5 shows the depth profile of the carbon concentration in a 5-nm thick HfSiO film as measured by SIMS. The amount of the C contaminant can be reduced by extending the O<sub>3</sub> treatment time. A light O<sub>3</sub> treatment for just 2s/cyc reduces the C concentration down to 2x10<sup>20</sup> atoms/cm<sup>3</sup> for both co-injection and lamine films.

We then investigated the electrical properties of HfSiON films with a Hf concentration of 55%. Figure 6 shows the I-V characteristics of N- and P-FETs with HfSiON gate dielectrics that were formed by the co-injection and lamine processes. The gate leakage current (J<sub>G</sub>) of the N-FETs and the threshold voltage (V<sub>TH</sub>) of the P-FETs are shown in Figures 7 and 8 as a function of the Equivalent Oxide Thickness (EOT). Figure 7 shows that the EOT increases as the O<sub>3</sub> treatment time is extended due to the growth of an interfacial layer. It is also noticeable that the J<sub>G</sub> values of the co-injection films are smaller than those of the lamine films, when they are compared at the same EOT. The higher J<sub>G</sub> of the lamine film is probably due to a reaction of the Hf in the film with the poly-silicon electrode [4], as implied by the higher V<sub>TH</sub> of the P-FET with the lamine film (Figure 8). This may be due to the existence of thin HfO<sub>2</sub> layers in the lamine film, as depicted in Figure 9. We assume that some interaction occurs between the Hf in the topmost HfO<sub>2</sub> layer and the poly-Si electrode across the thin SiO<sub>2</sub> layer. The co-injection film also shows superior immunity against PBT stress, as shown in Figure 10. It can be seen that the slope of ΔV<sub>TH</sub> is constant, regardless of the film structure, and that the offset depends on it. This means that there are more pre-existing traps in the lamine films, which may be also due to the HfO<sub>2</sub> layer in the film. PBTI and NBTI lifetime extrapolations are shown in Figures 11 and 12, respectively (ΔV<sub>TH</sub>=30mV). The co-injection film shows longer lifetimes for both PBTI and NBTI, which exceeds 10 years at V<sub>G</sub>=±1.0V. Prolonged O<sub>3</sub> treatment shows little impact on improving the lifetime, although the C concentration is reduced as shown in Figure 5. These results indicate that the slightest O<sub>3</sub> treatment (2s/cyc) is enough to maximize the film properties. Electron and hole mobilities are shown in Figure 13. Both co-injection and lamine films exhibit excellent values, 80% of universal at E<sub>EFF</sub>=0.8MV/cm. Finally, the EOT vs J<sub>G</sub> relationship for N-FETs with thin HfSiON gate dielectrics formed by the co-injection process with 2s/cyc O<sub>3</sub> treatment is shown in Figure 14. A TaSiN electrode was used for these samples alone. EOT scalability down to 0.86 nm with keeping J<sub>G</sub> lower than 36-nm-node targets [5] is confirmed. Performance of the PLCVD process and properties of the HfSiON films are summarized in Table 1 with those of the ALD process as comparison.

### 4. Conclusion

We have confirmed superior productivity of the PLCVD process compared to the ALD process, together with sufficient uniformity and controllability, as shown in Table 1. The co-injection process was superior to the lamine process in throughput, J<sub>G</sub> and reliability. Sufficient mobilities, BTI lifetimes over 10 years and EOT scalability down to 0.86 nm with keeping sufficient low J<sub>G</sub> were confirmed by the optimized condition. These results confirm that this method provides excellent manufacturability for 36-nm-node and further LOP and LSTP applications.

### References

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- [3] T. Nabatame et al, Symp. VLSI Tech. (2003) p.25.
- [4] S. Kamiyama et al, APL 86 (2005) p. 222904.
- [5] International Technology Roadmap for Semiconductor 2006.

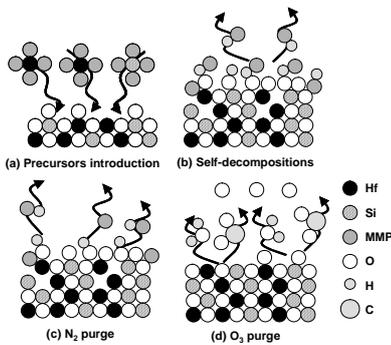


Fig. 1 Schematic of PLCVD process.

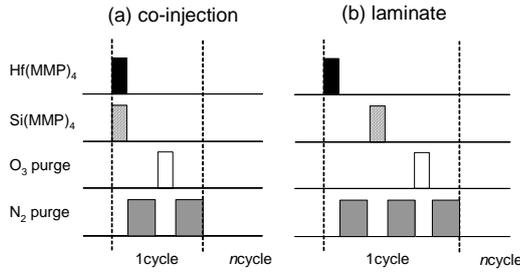


Fig. 2 Supply sequences for the co-injection process (a) and the laminate process (b).

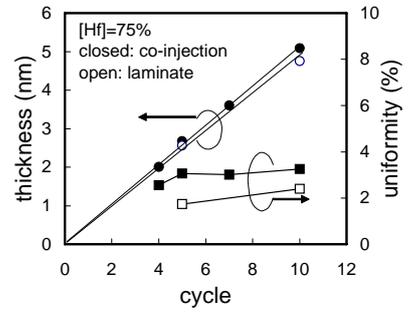


Fig. 3 Average thickness and thickness uniformity as a function of the number of process cycles.

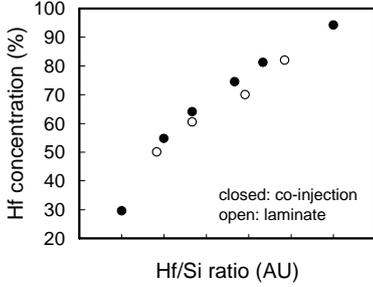


Fig. 4 Hf concentration in the PLCVD HF-silicate as a function of Hf and Si flow ratio (co-injection) or injection time ratio (laminate).

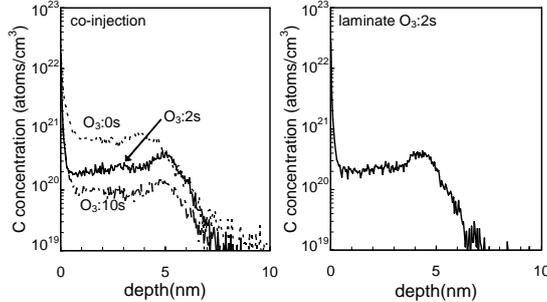


Fig. 5 Depth profiles of carbon concentration in 5-nm thick HfSiO films prepared by the co-injection (left) and laminate (right) processes, as measured by SIMS.

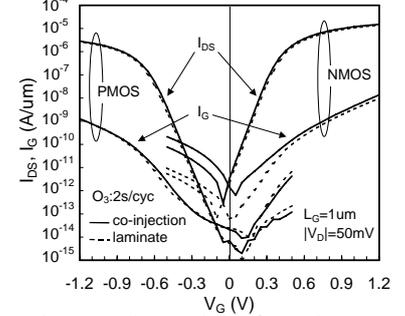


Fig. 6 I-V characteristic of N and P-FET with HfSiON gate dielectrics prepared by co-injection and laminate processes.

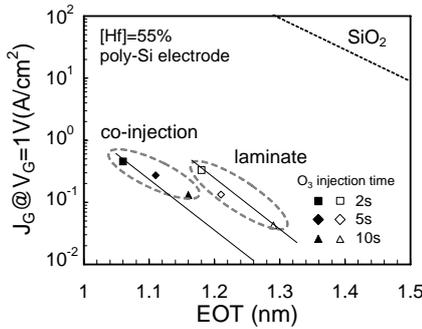


Fig. 7 EOT versus  $J_G$  for the HfSiON films formed by co-injection and laminate processes.

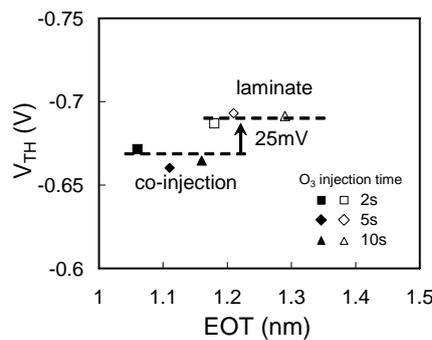


Fig. 8  $V_{TH}$  of PFETs with HfSiON gate dielectric formed by co-injection and laminate processes.

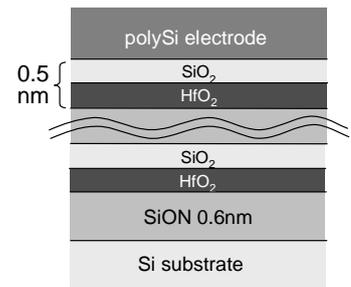


Fig. 9 Assumed film structure of HfSiO film formed by the laminate process.

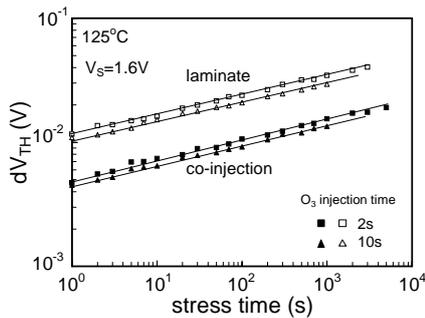


Fig. 10  $V_{TH}$  shift of the co-injection and the laminate films as a function of PBT stress.

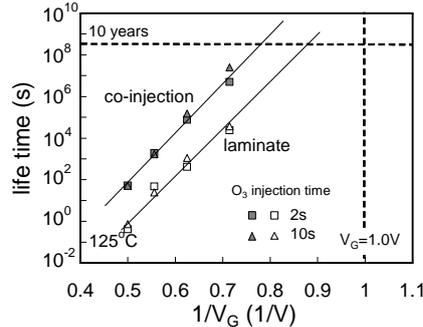


Fig. 11 PBTI lifetime extrapolation of co-injection and laminate films.

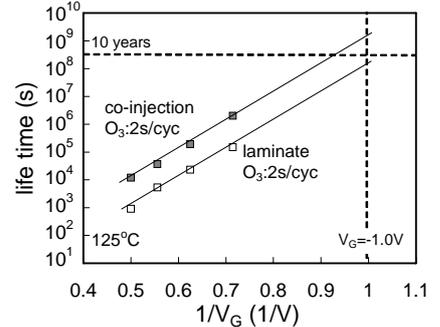


Fig. 12 NBTI lifetime extrapolation of co-injection and laminate films.

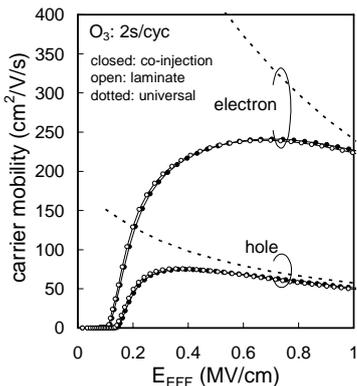


Fig. 13 Electron and hole mobilities of co-injection and laminate films.

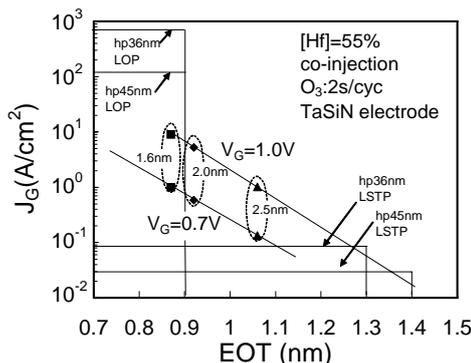


Fig. 14 EOT versus  $J_G$  at 0.7 and 1 V for thin HfSiON films formed by an optimized process. Physical thicknesses of HfSiON films are indicated.

	PLCVD (co-injection)	PLCVD (laminate)	ALD [2]
Growth rate (nm/cycle)	0.5	0.5	0.1
Number of process steps per cycle	4	6	4
Uniformity (%)	2.6	1.7	<3
Hf composition	30-100%	30-100%	0-100%
C conc. (cm <sup>-3</sup> )	2x10 <sup>20</sup>	2x10 <sup>20</sup>	<2x10 <sup>20</sup>
Mobility (% of universal)	80	80	80
$J_G$ @ 1.1nm, 1V (A/cm <sup>2</sup> )	0.23	1.7	0.17
PBTI lifetime (years)	6x10 <sup>4</sup>	3x10 <sup>3</sup>	-
NBTI lifetime (years)	48	4	-

Table 1. Summary of performance of the PLCVD and ALD processes and physical/electrical properties of HfSiON films by these processes.