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Highly Manufacturable CMOSFETs with Single High-*k* (HfLaO) and Dual Metal Gate Integration Process

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1. Introduction

Metal gate/high-k (MG/HK) technology would be required in sub-45 *nm* node CMOS devices [1-6], however it still suffers from high charge trapping and BTI degradation [7], low channel mobility [8], high V_{th} of the FETs due to Fermi level pinning (FLP) effect between MG and HK [9,10], as well as thermal reaction between HK and p-type metal [11,12]. Recently, it is reported that the incorporation of La into HfO_2-based gate dielectrics in MOS devices leads to superior device characteristics, in terms of BTI degradation, mobility and V_{th} [13-18]. However, most of the reports were for nMOSFETs demonstration only. Although Pt and Ir_3Si have been shown to possess a very high effective work function (EWF) on HfLaO (or HfLaON), a CMOS compatible integration scheme is still lacking for these gate materials. In this work, by using HfLaO dielectric, we demonstrate for the first time that the MG's EWF can be modulated continuously from 3.9 *eV* to 5.2 *eV* by controlling the thicknesses of p-type metal Ru and n-type metal TaN in a bilayer gate electrode. We also propose a highly manufacturable CMOS process scheme, in which these gate stack materials are integrated without degrading the underlying dielectric layer and/or channel region.

2. Experimental

N- and p-Si (001) substrates with background doping of $6x10^{15}cm^{-3}$ were used in the fabrication of MOSCAPs and MOSFETs in this work. The EWF tunability for the TaN/Ru stack was evaluated with MOSCAPs. The bottom metal layer Ru with varying thicknesses (from 2 *nm* to 50 *nm*) was deposited on HfLaO (Hf:La=1:1) by DC sputtering in a physical vapor deposition (PVD) tool, where HfLaO deposition technology can be found elsewhere [13]. Subsequently, the top metal layer TaN (150 *nm*) was deposited in-situ by reactive sputtering. MOSCAPs with a single metal layer, pure Ru (50 or 100 *nm*) or TaN (150 *nm*), were also fabricated for comparison. Following gate patterning, all devices were subjected to rapid thermal annealing (RTA) at different temperatures up to 1000°C for thermal stability evaluation. For MOSFETs, source/drain were implanted with BF_2 (50 *keV*, $1x10^{15}$ cm^{-2}), followed by RTA activation at 1000°C for 5 s. All samples received a backside Al metallization and forming gas annealing at 420 °C for 30 min.

3. Results and Discussion

(a) Electrical and Physical Characteristics:

Figure 1 shows the plot of V_{fb} versus EOT for pure Ru metal on HfLaO after 1000°C annealing. The low dependence of V_{fb} with varying EOT implies that there is a very low fixed charge density near the interface between HfLaO and the Si channel. However, the contribution of charges in HfLaO near the gate cannot be ruled out when explaining the observed difference in V_{fb}. Still, it is unlikely that any modification of fixed charges by Ru would be significantly different from the modification by TaN (see the inset of **Fig. 1**). Therefore, the changes of V_{fb} for these gate stacks are mainly due to the changes of metal EWF. In addition, based on the V_{fb} values on Si substrate with $6x10^{15}$ cm^{-3} doping concentration, we show evidence that incorporating La to HfO_2 can release the FLP between MG and HfO_2, causing EWF shifts from midgap 4.64 *eV* [2] to 5.2 *eV* for p-type metal Ru, and from 4.4 *eV* [13] to 3.9 *eV* for n-type metal TaN. A specific model based on the interfacial dipole theory between different MGs and HfLaO was proposed to illustrate this phenomenon [19]. **Figure 2(a)** depicts *CV* curves with different Ru thicknesses for TaN/Ru stack after high temperature annealing. The trend of V_{fb} shifts suggests the EWF of gate electrode increases with increasing the Ru thickness. This is quite similar to that reported in [20]. **Figure 2(b)** shows the V_{fb} change of a TaN/Ru gate stack with 100 *Å* Ru after different temperature annealing. The EWF decreased dramatically with the increase of annealing temperature. However, the constant V_{fb} shift after two subsequent 1000°C anneal suggests that the EWF changes after high temperature annealing are permanent. Transfer curves of pMOSFETs with the TaN/Ru/HfLaO gate stack are summarized in **Fig. 3(a)**, demonstrating around ~1.3 *V* V_{th} variation with the change of Ru thickness, consistent with the data from MOSCAPs. In addition, the comparable output curves for pure TaN, pure Ru and TaN/Ru stack are shown in **Fig. 3(b)**. **Figure 4** shows the energy dispersive X-ray spectroscopy (EDX) results of as deposited and 1000°C annealed TaN/Ru bi-layer stack. Ta was partially intermixed with Ru after 1000°C annealing, which was probably the root cause for the EWF change.

(b) Integration Scheme for CMOS Technology:

Based on the above results, a proposed integration process flow for CMOS with dual MG is shown in **Fig. 5**, whereby a single HK layer (HfLaO) was used without being exposed during the process. In addition, the selectivity of etching rate between Ru and TaN in both dry etch (as shown in **Fig. 6**) and wet etch ambient (hot SC-1 solution, data as shown in **Table 1**) was investigated, which indicates a simple method to integrate such dual MGs. AFM picture of as-deposited Ru is compared with those of Ru layers with the top TaN layer removed by wet etch and dry etch methods. The results shown in **Fig. 7** indicate there is negligible physical damage to the original thin Ru layer during the TaN etching process. In addition, the XPS analysis, shown in **Fig. 8**, indicates minimal TaN residue after etching process and no significant influence on chemical bond change for the original Ru layer. Electrical characteristics for MOS devices among the simple deposition and re-deposition Ru layer after wet etch and dry etch TaN layer first were compared in **Figs. 9(a)**, **(b)** and **(c)**. It was confirmed that there was no obvious damage to the underlying HK layer during the process for removing the TaN layer. All of these results show that TaN/Ru (for nMOSFETs) and Ru (for pMOSFETs) on HfLaO gate stacks are promising candidates for future CMOS integration technology.

4. Conclusions

In this work, we first demonstrate that by employing TaN/Ru on HfLaO gate stacks with different Ru thicknesses, the metal EWF can be tuned continuously with a wide range from n-type band-edge (3.9 *eV*) to p-type band-edge (5.2 *eV*). In addition, we also propose and demonstrate a very highly manufacturable CMOS integration process for these gate stacks.

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Reference

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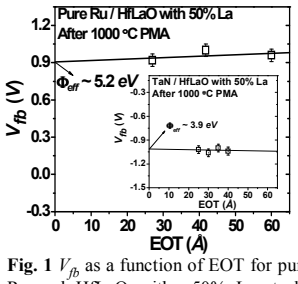


Fig. 1 V_{fb} as a function of EOT for pure Ru and HfLaO with ~50% La stacks after 1000ºC annealing, the inset shows the case of TaN/HfLaO stacks.

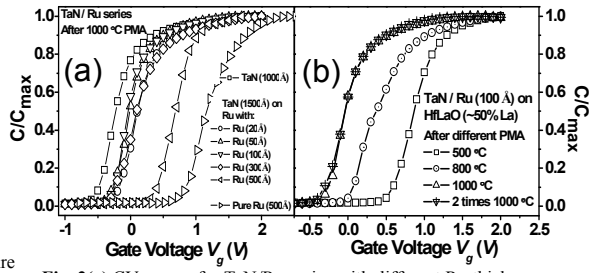
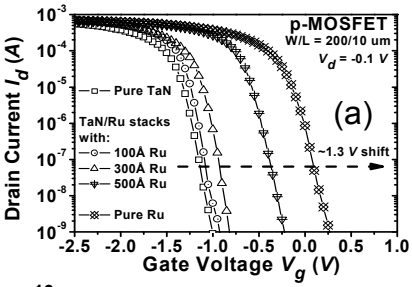


Fig. 2(a) CV curves for TaN/Ru series with different Ru thicknesses after high temperature annealing and **(b)** TaN/Ru with 100Å Ru after different temperature RTA.



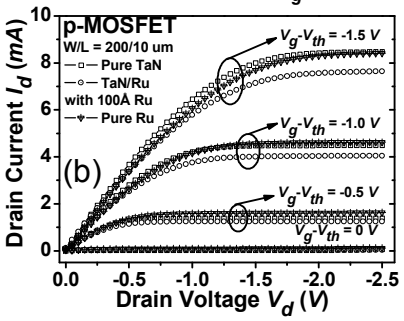


Fig. 3(a) Transfer characteristics of pMOSFETs with TaN/Ru gate stacks. Different Ru thicknesses introduce ~1.3 *V* V_{th} shift; **(b)** Output characteristics of pMOSFETs with pure TaN, TaN/Ru stack with 100 Å Ru and pure Ru metal gate after 1000 ºC annealing.

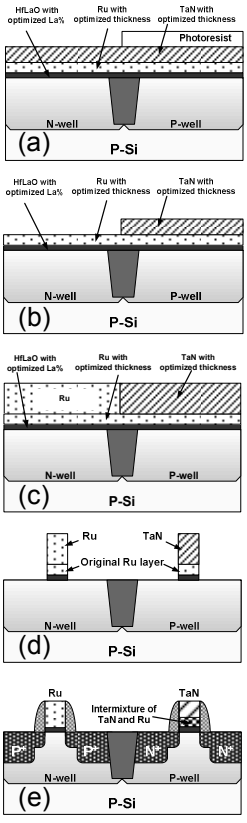


Fig. 5(a)-(e) Schematic illustration of the process flow for possible dual metal gate CMOS integration.

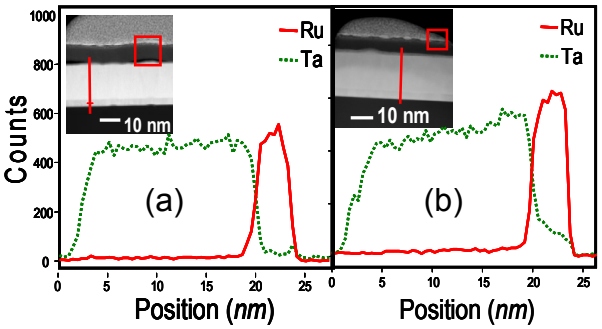


Fig. 4 EDX analysis for TaN and Ru stack, (a) As deposited and (b) After 1000ºC 5 sec RTA. Obvious Ta diffusion into Ru layer up to the interface between Ru and HfLaO was observed after high temperature annealing.

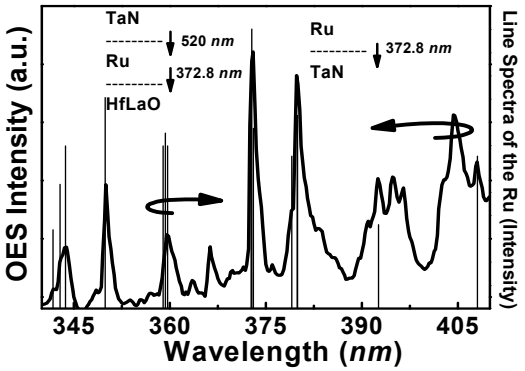


Fig. 6 Optical Emission Spectra (OES) intensities detected during etching of Ru gate stack in O_2 plasma, line spectra of the Ru elements also shown on the right axis. The endpoint of TaN, etched in Cl_2 plasma is obtained using 520 *nm* wavelength. When Ru is exposed to Cl_2 plasma, Ru film is not etched due to formation of nonvolatile $RuCl_x$. Moreover, when HfLaO film is exposed to O_2 plasma, the high-*k* film is not etched.

Table 1 Selectivity of TaN and Ru in hot SC-1 ($NH_4OH+H_2O_2+H_2O$).

Solution	Etching rate (*nm/min*)	
	TaN	Ru
Hot SC-1	~16	0

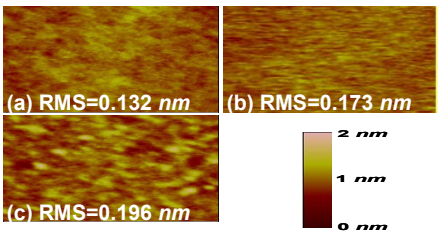


Fig. 7 AFM pictures for pure Ru film (a), TaN/Ru stacks after TaN etching in both dry and wet mode, respectively (b) & (c). 0.064 *nm* variation of RMS indicates negligible physical damage to the original Ru layer during the etch processes.

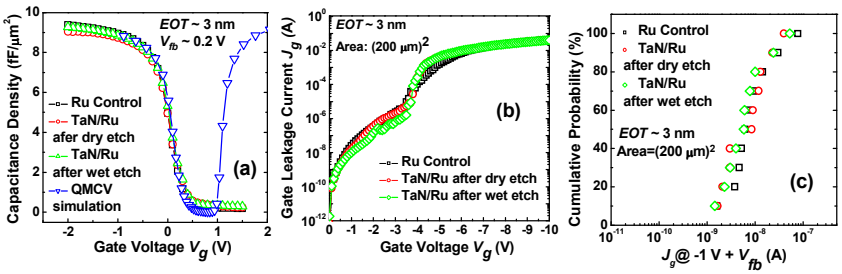


Fig. 9 Comparison of *C-V* characteristic (a), J_g-V_g characteristic (b) and J_g distribution @ V_{fb}-1V among the Ru control devices and re-deposited Ru layer after removal of TaN layer by dry etch and wet etch respectively.

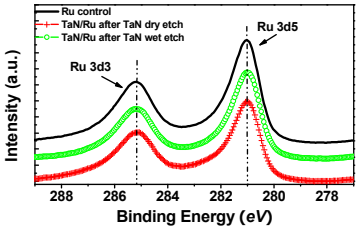


Fig. 8 XPS spectra of Ru 3d taken from pure Ru film, TaN/Ru stacks after TaN etching in both dry and wet mode. The consistent spectra indicate minimal TaN residue after etch process and no significant influence on chemical bond change for the originally underlying Ru layer.