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Highly Manufacturable and Cost-effective Single Ta_xC / $Hf_xZr_{(1-x)}O_2$ Gate CMOS Bulk Platform for LP Applications at the 45nm Node and Beyond

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1. Introduction

Industrially viable metal gate / High-K solutions are urgently needed in order to assure the gate capacitor scaling in future CMOS technology nodes. Over the past years good progress has been made in both the material engineering and the integration of dual metal gate and High-K [1-4]. However, the choice of a gate–first compatible p-like gate electrode is still a big issue and few papers report on well adjusted PMOS threshold voltages (VT) [5-7]. The alternative Totally Silicided gate approach - very appealing on SiON - requires a dual silicide process on High-K to meet the work function (WF) targets adding thus substantial integration complexity [8-11]. A very pragmatic solution is the combination of a single N-like metal gate with a buried channel by B counterdoping (C-Dope) in the PMOS as it has been proposed in ref. [12] on PDSOI in a high performance perspective. In this paper, we will show that this option is also applicable for bulk CMOS LP applications reporting on excellent device, circuit and reliability results obtained on 300mm.

2. Device Fabrication and Morphology

Devices are fabricated in a CMOS flow on <100> substrates with (001) channel orientation. For the gate stack, a layer of 20Å (25Å) $Hf_xZr_{(1-x)}O_2$ has been deposited on a chemical oxide surface, capped by 10nm Ta_xC and 100nm poly-Si. After gate patterning - the nominal gate length is 40nm - nitride offset spacers are formed. After the LDD implantation, spacer formation and S/D implantation, a spike anneal was performed (Fig. 1). Devices have a tensile nitride contact etch stop layer. Fig. 2 shows the cross section of a 33nm-long device with a zoom on the gate stack.

3. Gate Stack and Device Characteristics

Fig. 3 shows the C-V curves of 100µm² devices. For the NMOS we find 14.6 (14.9) Å CET_{inv} for Jg = 0.12 (0.07) A/cm² for the 20 (25) Å thin $Hf_xZr_{(1-x)}O_2$ (Fig 4). This corresponds to 9Å *CETinv* reduction compared to a state-of-the-art poly-Si/SiON 45nm LP technology at equal gate leakage [13]. PMOS devices have 2.5Å higher CET_{inv} values due to the buried channel. Electron mobility is slightly better on the thinner oxide where the high effective field mobility is close to the universal curve (Fig. 5). The B counter-doping lowers the long channel VT from initially 0.8V to 0.1V for the strongest C-Dope recipe enabling to match the PMOS VT perfectly to the NMOS VT of 0.45V, while the VT dispersion stays well controlled over a wide range (Fig. 6 to 8). Static performances are competitive with best values I_{on} = 755(780) / 305(295) µA/µm for I_{off} = 1nA/µm at V_{dd}=1.1V for the 20Å (25Å) thin $Hf_xZr_{(1-x)}O_2$ on nominal N/PMOS and outperform the results of the 45nm LP poly-Si/SiON platform in ref. [13] thanks to the aggressive CET_{inv} scaling (Fig. 9 and 10).

4. SRAM Assessment and Reliability

For full assessment of our single metal $Ta_xC/Hf_xZr_{(1-x)}O_2$ approach, CMOS devices have been integrated into 0.499µm² SRAM cells (cf. Fig. 11-14). The butterfly curves are symmetrical and the Static Noise Margin (SNM) values reach 203 ± 19 mV at V_{dd} = 1.1V for the thinner oxide. The Write Margins (WM) are good with 358 ± 54 mV on the same split. The standby and read currents are 14pA and 15µA per cell respectively. The excellent SRAM results are reflected by low NMOS VT mismatch values: only 2.8mV.µm is observed for the 20Å $Hf_xZr_{(1-x)}O_2$, which can be attributed to both the metal gate and the aggressively scaled CET_{inv} (Fig. 15). Fig. 16 shows a comparison of the major device and SRAM characteristics with recent literature data. Our results are among the best SRAM data obtained with advanced gate stacks. The reliability of the $Ta_xC/Hf_xZr_{(1-x)}O_2$ stack is assessed via NBTI lifetime measurements and compared to TiN-gated references using the "on-the-fly-method" (ΔVT_{max}=50mV, T= 125°C) [14]. Fig. 17 shows that the use of the Ta_xC gate electrode results in a significant lifetime increase. Moreover, the 10 year lifetime criterion is easily met for both oxide thicknesses at V_g = 1.1V, targeted for LP applications. These results confirm the good BTI results of the $Ta_xC/Hf_xZr_{(1-x)}O_2$ stack reported in ref. [3]. TDDB measurements were carried out for both Ta_xC /$Hf_xZr_{(1-x)}O_2$ gate stacks using a 0.1% failure rate criterion on a 0.1cm² surface at 125°C. The extrapolation of the data points gives a maximum gate voltage corresponding to 10 years lifetime of 1.29V (1.06V) for the 25Å (20Å) thin $Hf_xZr_{(1-x)}O_2$ indicating that the reliability requirements can be met (Fig. 18).

5. Conclusion

In this paper, we have demonstrated the manufacturability of a cost-effective single metal Ta_xC on $Hf_xZr_{(1-x)}O_2$ CMOS bulk approach for future LP applications. The use of a buried channel - engineered by B counterdoping - enables perfectly symmetric VTs down to 30nm gate length and very competitive device results. Device dispersion is well controlled leading to excellent 0.499µm² SRAM results with mean values of 203mV (358mV) SNM (WM) at V_{dd} = 1.1V. The choice of Ta_xC and $Hf_xZr_{(1-x)}O_2$ for the gate stack is justified by very low VT mismatch values and good reliability behaviour making this approach a valid candidate for future LP applications.

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[1] J. Schaeffer et al., *IEDM*, p. 287, 2004; [2] S. Inumiya et al., *IEDM*, p. 28, 2005; [3] R. Hegde et al., *IEDM*, p. 39, 2005; [4] S. Samavedam et al., *IEDM*, p. 307, 2003; [5] P. F. Hsu et al., *VLSI*, p. 14, 2006; [6] S. C. Song et al., *VLSI*, p. 16, 2006; [7] K. Singanamalla et al., *IEDM*, p.43, 2006; [8/9] M. Müller et al ., *IEDM*, p. 641, 2005 and *SSDM*, p. 1108, 2006; [10] A. Mondot et al., ESSDERC, p. 117, 2006; [11] T. Hoffmann et al., p. 2006 ; [12] W. J. Taylor et al., *IEDM*, p. 625, 2006 ; [13] E. Josse et al., *IEDM*, p. 693, 2006 ; [14] V. Huard et al., *IRPS*, p.733, 2006 ; [15/16] A. Vandooren et al., *SOI Conf. Proc.*, p. 221, 2005 and *IEDM*, p. 975, 2003; [17] H. Nakamura et al., *VLSI*, p. 198, 2006; [18] B. Doris et al., *VLSI*, p. 214. 2005.

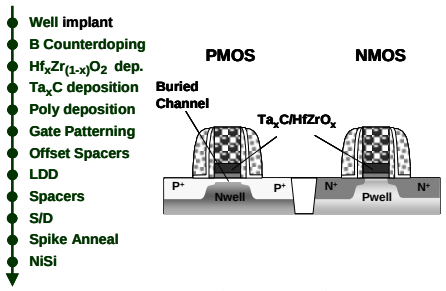

Fig. 1: CMOS integration of the Ta_xC /$Hf_xZr_{(1-x)}O_2$ gate stack with PMOS B counterdoping

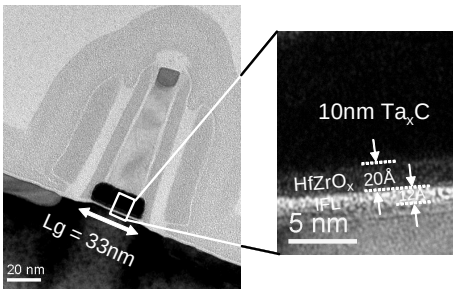

Fig. 2 : TEM micrograph of a 33nm Ta_xC/20Å $Hf_xZr_{(1-x)}O_2$ device.

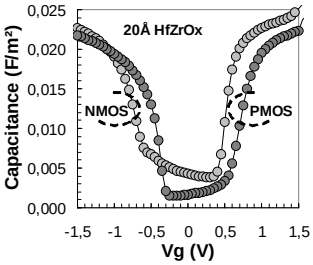

Fig. 3: Capacitance curves of 10µm*10µm N- and PMOS devices (20Å $Hf_xZr_{(1-x)}O_2$).

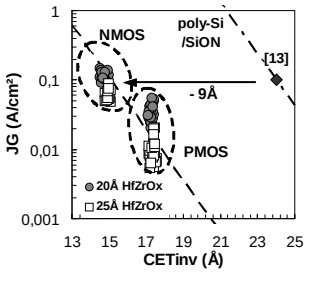

Fig. 4: Gate Leakage versus CET_{inv}.

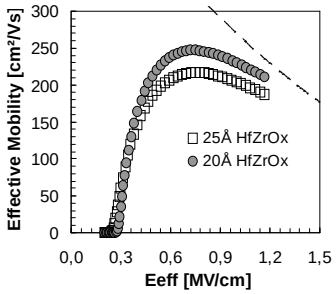

Fig. 5: Effective electron long channel mobility.

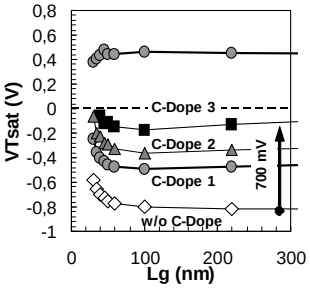

Fig. 6: PMOS Threshold Voltage adjustment by B Counter-doping.

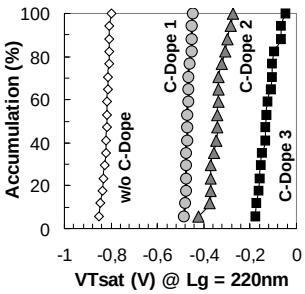

Fig. 7: Threshold Voltage dispersion for B-counterdoped PMOS devices (220nm).

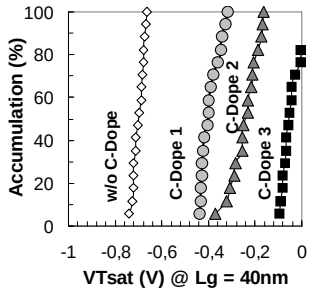

Fig. 8: Threshold Voltage dispersion for B-counterdoped PMOS devices (40nm)

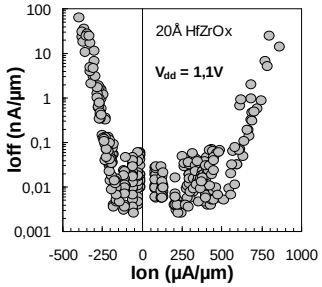

Fig. 9: CMOS performance for 20Å $Hf_xZr_{(1-x)}O_2$.

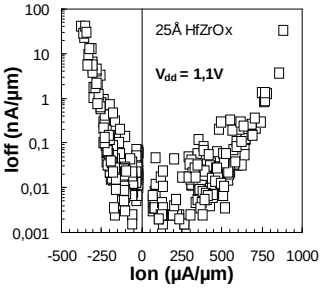

Fig. 10: CMOS performance for 25Å $Hf_xZr_{(1-x)}O_2$.

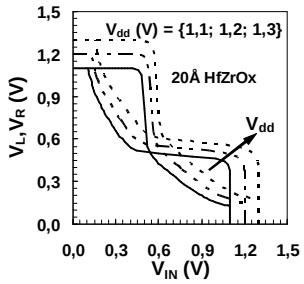

Fig. 11: Butterfly curves of 0.499µm² SRAM cells (L_g = 40nm).

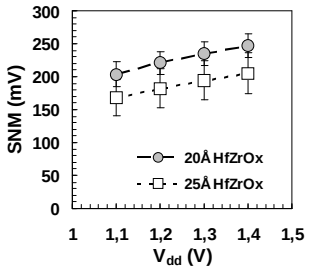

Fig. 12: SRAM Static Noise Margin as a function of Vdd.

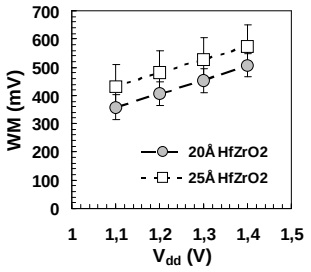

Fig. 13: SRAM Write Margin as a function of Vdd.

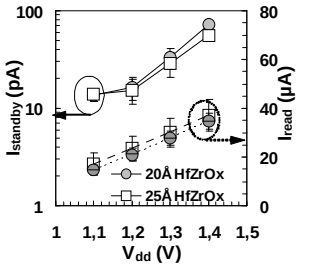

Fig. 14: SRAM standby and read currents as a function of Vdd.

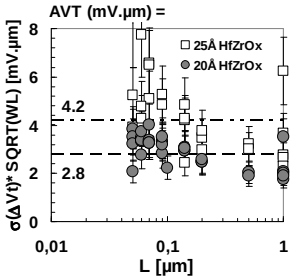

Fig. 15: Normalised NMOS VT mismatch.

Reference	This paper		[13]	[17]	[12]	[5]	[15]	[18]
N / P-Gate	Ta_xC	Ta_xC	poly	poly	TaC	TaC/MoN	TiN	MeN/MeN
Gate Oxide	20Å $HfZrO_x$	25Å $HfZrO_x$	SiON	HfSiON	HfZrO2	HfO2	HfO2	HfO2
Specificities	tCESL	tCESL	tSTI, tCESL RTA+Laser	stress by STI, CESL	PDSOI, DSL	CESL	FDSOI	FDSOI
Vdd (V)	1.1	1.1	1.1	1.2	1.2	1.2	1.2	1.3
CETinv (Å)	15/17	15/17	24/25.5	26.5	16/18*	16/18.5	20	14
Jg (A/cm²)	0.13/0.04	0.07/0.01	0.1/-	0.05	0.1/0.008*	4/0.2	-	0.5
Lg (nm)	40	40	42	50	40	55	45	50
Vtsat (V)	0.43/ 0.40	0.33/ 0.40	-	0.35/0.35	0.15/0.5*	0.3/0.45	0.4/0.3	0.1/0.5
Ion (µA/µm)	755 / 305	780 / 295	630/ 320	640/340	1150 / 570	700/390	400/300*	1050/770
Ioff (µA/µm)	1	1	1	0.2	1	0.2	1	28
SRAM size (µm²)	0.499	0.499	0.37	-	0.64	-	0.53	2.6
SNM (mV)	203	169	180	180	190	-	275	330
WM (mV)	360	420	-	-	-	-	460	-
I_read (µA/cell)	14.7	17.3	-	-	80	-	10	-
I_stby (pA/cell)	13.7	13.8	-	-	-	-	543	-
A_{VT} NMOS (mV.µm)	2.8	4.2	3.4	-	-	-	2.9 [16]	-
					* @ 1V		* @ 1V	

Fig. 16 : Comparison of device and SRAM results to recent publications.

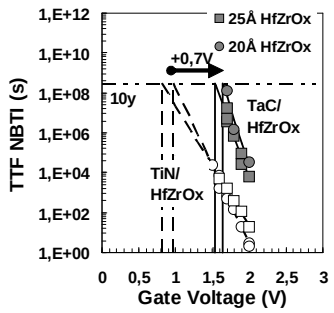

Fig. 17: NBTI lifetime for Ta_xC and TiN gated devices w/ $Hf_xZr_{(1-x)}O_2$ gate oxide.

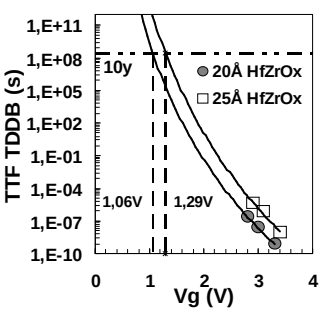

Fig. 18: Time Dependent Dielectric Breakdown for Ta_xC on $Hf_xZr_{(1-x)}O_2$.