Highly Manufacturable and Cost-effective Single Ta/C / Hf(Zr,C)/SiO₂ Gate CMOS Bulk Platform for LP Applications at the 45nm Node and Beyond


NXP Semiconductors, Freescale, STMicroelectronics, 850 rue Jean-Monnet, F-38920 Crolles Cedex, France

1. Introduction

Industrially viable metal gate / High-K solutions are urgently needed in order to assure the gate capacitor scaling in future CMOS technology nodes. Over the past years good progress has been made in both the material engineering and the integration of dual metal gate and High-K [1-4]. However, the choice of a gate-first compatible p-like gate electrode is still a big issue and few papers report on well adjusted PMOS threshold voltages (VT) [5-7]. The alternative Totally Silicided gate approach - very appealing on SiON - requires a dual silicidic process on High-K to meet the work function (WF) targets adding thus substantial integration complexity [8-11]. A very pragmatic solution is the combination of a single N-like metal gate with a buried channel by B counterdoping (C-Dope) in the PMOS as it has been proposed in ref. [12] on PDSOI in a high performance perspective. In this paper, we will show that this option is also applicable for bulk CMOS LP applications reporting on excellent device, circuit and reliability results obtained on 300nm.

2. Device Fabrication and Morphology

Devices are fabricated in a CMOS flow on <100> substrates with (001) channel orientation. For the gate stack, a layer of 20Å (25Å) Hf(Zr,C)/SiO₂ has been deposited on a chemical oxide surface, capped by 10nm Ta/C and 100nm poly-Si. After gate patterning - the nominal gate length is 40nm - nitride offset spacers are formed. After the LDD implantation, spacer formation and S/D implantation, a spike anneal was performed (Fig. 1). Devices have a tensile nitride contact etch stop layer. Fig. 2 shows the cross section of a 33nm-long device with a zoom on the gate stack.

3. Gate Stack and Device Characteristics

Fig. 3 shows the C-V curves of 100μm devices. For the NMOS we find 14.6 (14.9) A/CTEₜₐₜ for Iₜ = 0.12 (0.07) A/cm² for the 20 (25) Å thick Hf(Zr,C)/SiO₂ (Fig. 4). This corresponds to 9Å C/ETₜₐₜ reduction compared to a state-of-the-art poly-Si/SiON 45nm LP technology at equal gate leakage [13]. PMOS devices have 2.5Å higher C/ETₜₐₜ values due to the buried channel. Electron mobility is slightly better on the thinner oxide where the high effective field mobility is close to the universal curve (Fig. 5). The C-D counterdoping lowers the long channel VT from initially 0.8V to 0.1V for the strongest C-Dope recipe enabling to match the PMOS VT perfectly to the NMOS VT of 0.45V, while the VT dispersion stays well controlled over a wide range (Fig. 6 to 8). Static performances are competitive with best values Iₜₐₜ = 755/780 / 305/295 μA/mm for Iₜ = 1nA/mm at Vₓₛ=1.15V for the 20Å (25Å) thick Hf(Zr,C)/SiO₂ on nominal NPMOS and outperform the results of the 45nm LP poly-Si/SiON platform in ref. [13] thanks to the aggressive C/ETₜₐₜ scaling (Fig. 9 and 10).

4. SRAM Assessment and Reliability

For full assessment of our single metal Ta/C/Hf(Zr,C)/SiO₂ approach CMOS devices have been integrated into 0.49μm² SRAM cells (cf. Fig. 11-14). The butterfly curves are symmetrical and the Static Noise Margin (SNM) values reach 203 ± 19 mV at Vₓₛ = 1.1V for the thinner oxide. The Write Margins (WM) are good with 358 ± 54 mV on the same split. The standby and read current are 1μA and 15μA per cell respectively. The excellent SRAM results are reflected by low NMOS VT mismatch values: only 2.5nm/μm is observed for the 20Å Hf(Zr,C)/SiO₂, which can be attributed to both the metal gate and the aggressively scaled C/ETₜₐₜ (Fig. 15). Fig. 16 shows a comparison of the major device and SRAM characteristics with recent literature data. Our results are among the best SRAM data obtained with advanced gate stacks. The reliability of the Ta/C/Hf(Zr,C)/SiO₂ stack is assessed via NBTI lifetime measurements and compared to TiN-gated references using the “on-the-fly-method” (ΔVTₜₐₜ=50mV, T=125°C) [14]. Fig. 17 shows that the use of the Ta/C gate electrode results in a significant lifetime increase. Moreover, the 10 year lifetime criterion is easily met for both oxide thicknesses at Vₓₛ = 1.1V, targeted for LP applications. These results confirm the good BTI results of the Ta/C/Hf(Zr,C)/SiO₂ stack reported in ref. [3]. TDDM measurements were carried out for both Ta/C/Hf(Zr,C)/SiO₂ gate stacks using a 0.1% failure rate criterion on a 0.12μm² surface at 125°C. The extrapulation of the data points gives a maximum gate voltage corresponding to 10 years lifetime of 1.29V (1.06V) for the 25Å (20Å) thin Hf(Zr,C)/SiO₂ indicating that the reliability requirements can be met (Fig. 18).

5. Conclusion

In this paper, we have demonstrated the manufacturability of a cost-effective single metal Ta/C on Hf(Zr,C)/SiO₂ CMOS bulk approach for future LP applications. The use of a buried channel - engineered by B counterdoping - enables perfectly symmetric VTs down to 30nm gate length and very competitive device results. Device dispersion is well controlled leading to excellent 0.49μm² SRAM results with mean values of 20mV (35mV) SNM (WM) at Vₓₛ = 1.1V. The choice of Ta/C and Hf(Zr,C)/SiO₂ for the gate stack is justified by very low VT mismatch values and good reliability behaviour making this approach a valid candidate for future LP applications.

Acknowledgements

The authors would like to thank J. Schaeffer, B. Taylor, R. Hegde, A. Vandooren, J. Petry, C. Ravit, J. Hooker, F. Martin, and P. Mur for the helpful discussions. This research is partly supported by the European Commission’s Information Society Technologies Programme, under PULLNANO project contract No. IST-026828.

References


-852-
Fig. 8: Threshold Voltage dispersion for 20 Å HfZrOx.

Fig. 4: Gate Leakage versus Gate Oxide thickness for 20 Å HfZrOx.

Ioff (µA/µm) 1.1 1.0 0.9 0.8 0.7 0.6 0.5 0.4 0.3 0.2 0.1 0.0
Ion (µA/µm) 755 / 305 780 / 295 630/ 320 640/340 1150 /  570 700/390 400/300*

Lg (nm) 40 40 42 50 40 55 45 50

Vdd (V) 1.1 1.1 1.1 1.2 1.2 1.2 1.2 1.3

I_read (µA/cell) 14.7 17.3 -

I_stby (pA/cell) 13.7 13.8 -

Reference [13] [17] [12] [5] [15] [18]

This paper

Fig. 10: CMOS performance for 25 Å HfZrOx.

Fig. 12: SRAM Static Noise Margin as a function of Vdd.

Fig. 13: SRAM Write Margin as a function of Vdd.

Fig. 14: SRAM standby and read currents as a function of Vdd.

Fig. 15: Normalised NMOS VT mismatch.

Fig. 16: Comparison of device and SRAM results to recent publications.

-853-