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CMP-less Co-Integration of Tunable Ni-TOSI CMOS for Low Power Digital and Analog Applications

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1. Introduction

Among the different metallic gates integration options, the TOtal SIlicidation (TOSI) of initial poly-Si gates is regarded as a very pragmatic solution [1-6]. Especially, the CMP-less TOSI integration approach – based on the simultaneous silicidation of an ultra-low gate and epitaxially raised S/D areas – requires only few changes with respect to a CMOS standard flow and leads to full CMOS integration [5]. NiSi seems to be an ideal candidate for the gate silicidation as it is fully compatible with the junction requirements of scaled MOSFETs and as it offers the possibility of work function tuning by Silicidation Induced Impurity Segregation (SIIS) at the silicide / gate oxide interface when predoping the poly-Si prior to the gate silicidation process [7,8]. An important aspect for industrial application of CMOS technologies is to provide both core and I/O devices, ideally having the same gate electrode in order to avoid cost-intensive masking steps. In this paper we will focus on this topic presenting first a V_t-tunable NiSi-TOSI gate satisfying the reliability of the core devices and evaluating its suitability for the requirements of the cointegrated I/O devices in terms of performance, gain and matching behaviour.

2. Device Fabrication and Morphology

Fig. 1 illustrates the TOSI-gate integration scheme comprising GOx1 and GOx2 devices, based on the approach developed in ref. [5]. After formation of the GOx2 (50Å final thickness) and GOx1 (17Å EOT PNO SiON), 30nm poly-Si is deposited, which is - if not noted otherwise - pre-implanted by $3x10^{15}$cm-2 B (P) for PMOS (NMOS) devices and finally capped by an oxide hard mask. After gate patterning and LDD, halo and pocket implantations, the S/D areas are epitaxially raised before the S/D implantations. After the S/D anneal the hard mask is removed and the simultaneous silicidation of the gate down to the oxide and the junctions is carried out using a two step thermal treatment. Fig. 2 shows a final TOSI-gate GOx1 NMOS transistor with 34nm-gate length. The EFTEM analysis – sensitive to the different atomic species - confirms the complete silicidation of the gate.

3. Core Device Results

Fig. 3-4 summarise the effect of the gate implantation prior to gate silicidation: both B and P implantation yield a substantial and gate length scalable V_t lowering of 250mV with respect to the undoped midgap NiSi-TOSI-gate while the corresponding C-V curves prove the complete silicidation of the gate. Fig. 5 shows the well-behaved I_d-V_g characteristics of 35nm-short TOSI-gate PMOS and NMOS transistors. As seen in Fig. 6, the total gate silicidation offers a neat improvement in the J_g-CET_{inv} trade-off, stemming from the metallic character of the gate, without degrading the gate leakage current J_g in inversion. The GOx1 integrity after the TOSI process is confirmed by the excellent NBTI-results (cf. Fig. 7 and 8): the TOSI-gate devices exhibit the same slope as the poly-Si reference when plotted versus V_{ox} ruling out additional degradation mechanisms and their absolute lifetime exceeds the 10 years criterion for $V_g < 1.25$V.

4. I/O Device Results

Concerning GOx2 devices featuring the 50Å-thick SiON gate oxide (cf. Fig. 9), the V_t shift between the doped TOSI-gate devices and the poly-Si references is equivalent to that of the GOx1 devices, proving that the V_t adjustment is only gate electrode and not gate oxide related (cf. Fig. 10). The resulting device performances are shown in Fig. 11. The C-V curves of Fig.12 give evidence for the complete gate silicidation on the GOx2 devices. 1/*f* noise has been observed at low frequency and the normalized drain current spectral density S_{id}, plotted as function of V_g-V_t, exhibits similar behaviour for TOSI devices and poly-Si references excluding process related oxide trap density increase. The TOSI-gate process is found beneficial to the analog gain with a neat increase in the (P)-TOSI NMOS and equivalent gain for the (B)-TOSI PMOS devices (cf. Fig. 14). Both V_t and β mismatch measurements have been performed on 30 pairs of neighbouring GOx2 PMOS transistors. For higher accuracy, the corresponding matching parameters A_β have been extracted using a weighted regression method [9]. The (B)-TOSI 50Å GOx2 PMOS devices exhibit a normalised V_t mismatch of AV_t/T_{ox}[nm]=0.84mV.µm, which is slightly lower than the 1mV.µm value commonly observed on bulk technology [10], and the relative β-mismatch displays an acceptable value of A_β=3.2 %.µm (cf. Fig 15 and 16).

5. Conclusion

In this work, we have shown for the first time a successful cointegration of core and I/O devices displaying V_t-tunable NiSi TOSI gates fabricated in a CMP-less flow. The 17Å EOT SiON core devices demonstrate a V_t tunability of +/- 250mV by B and P gate predoping prior to silicidation down to 35nm gate length and excellent reliability results. The co-integrated 50Å SiON TOSI-gate I/O devices show good performances and matching characteristics and improved analog gain emphasizing clearly the potential of TOSI-gates as metal gate options for future CMOS technologies.

6. Acknowledgements

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7. References

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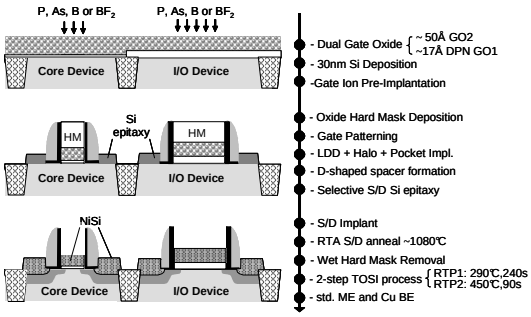

Fig. 1: CMP-less integration scheme and transistor flow of cointegrated GOx1 and GOx2 CMOS devices.

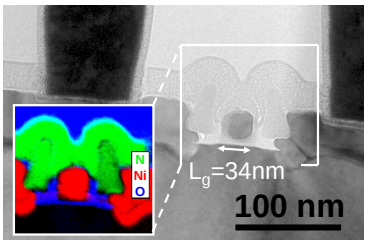

Fig. 2: TEM picture of a 34nm-short (P)-TOSI-gate GOx1 NMOS device, giving evidence for the complete gate silicidation (see EFTEM insert).

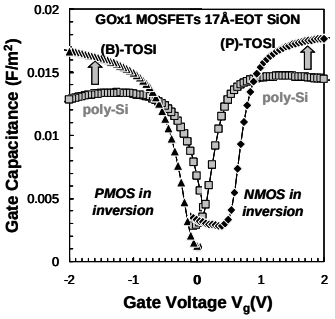

Fig. 3: Gate capacitance of GOx1 TOSI-gate MOSFETs vs. poly-Si ref.

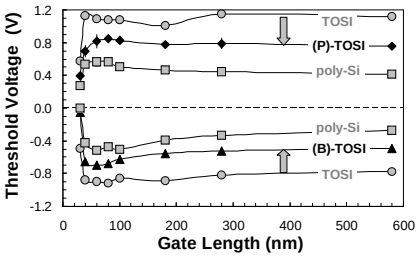

Fig. 4: Linear threshold voltage of TOSI-gate GOx1 N and PMOS devices with and without gate predoping.

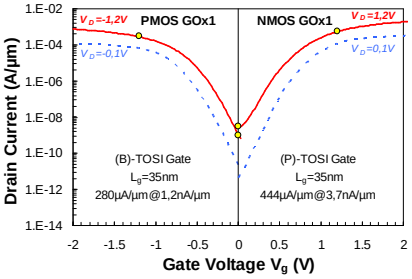

Fig. 5: Id(Vg) characteristics of GOx1 35nm-long (B)-TOSI PMOS and (P)-TOSI NMOS devices.

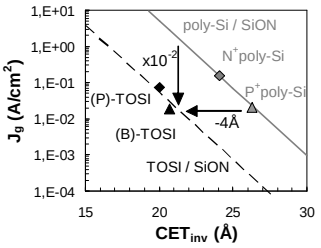

Fig. 6: Improvement of the J_g-CET_{inv} trade-off by the TOSI on GOx1 devices.

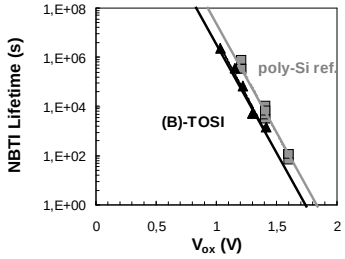

Fig. 7: Comparison of NBTI lifetime versus V_{ox} for (B)-TOSI-gate GOx1 PMOS devices and a poly-Si reference (ΔV_t =50mV @ 125°C).

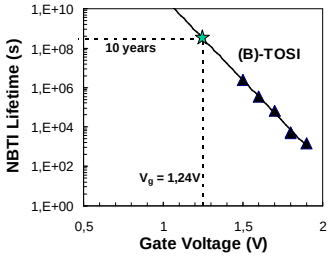

Fig. 8: NBTI lifetime extrapolation for (B)-TOSI-gate PMOS GOx1 devices (ΔV_t =50mV @ 125°C)

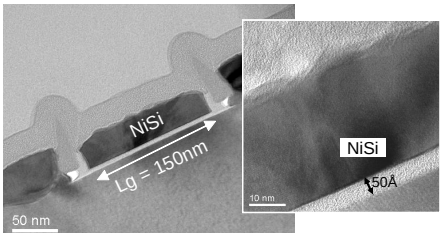

Fig. 9: TEM picture of a 150nm-long (B)-TOSI-gate 50Å EOT GOx2 device with zoom on gate oxide.

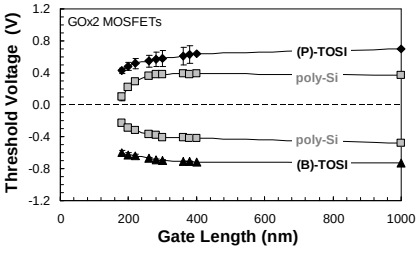

Fig. 10: Linear threshold voltage of GOx2 (B)-TOSI PMOS and (P)-TOSI NMOS devices compared to the corresponding poly-Si references.

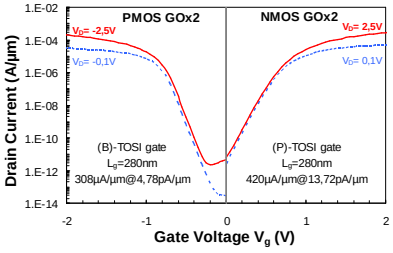

Fig. 11: I_d-V_g characteristics of GOx2 280nm-long (B)-TOSI PMOS and (P)-TOSI devices (V_{dd} = 2.5V).

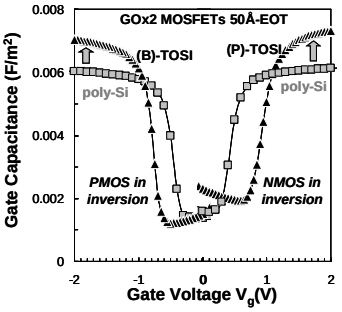

Fig. 12: Gate capacitance of GOx2 TOSI-gate MOSFETs vs. poly-Si ref.

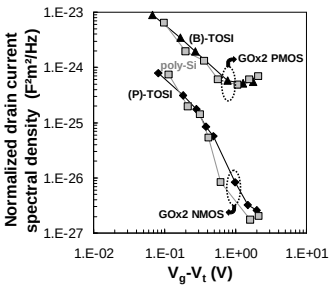

Fig. 13: Normalized LF noise level as a function of V_g -V_t.

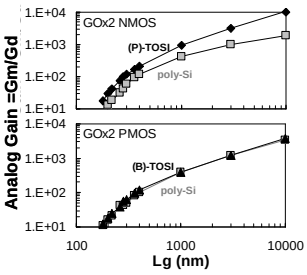

Fig. 14: Analog gain on GOx2 TOSI devices vs. poly-Si ref.

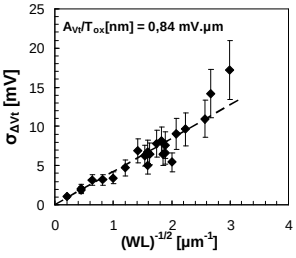

Fig. 15: Relative V_t-mismatch of (B)-TOSI gate GOx2 PMOSFETs.

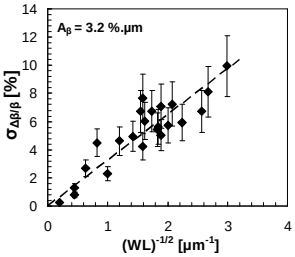

Fig. 16: Relative β-mismatch of (B)-TOSI gate GOx2 PMOSFETs.