Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 30-31

B-1-1 High mobility Ge channel metal source/drain pMOSFETs with nickel fully silicided gate

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Introduction

A Ge channel is an attractive technology booster for future high performance CMOS, because of its high mobility. However, low solubility and high diffusion constant of dopants in Ge make it difficult to fabricate the aggressively-scaled MOSFETs with low source/drain extension (SDE) resistance. In order to overcome these problems, we have proposed Metal (Germanide) Source/ Drain (MSD) Ge channel MOSFETs [1,2] which offer low SDE resistance. On the other hand, gate stack formation on Ge is another key issue to realize the high performance devices. There have been some reports on high-k gate insulators and metal gates on Ge [3, 4] and high channel mobility has been reported in pMOSFETs using TaN/HfO_2 gate stack with Si surface passivation [4]. However, V_{th} control has not been taken into account in the previous devices. In this paper, we propose a novel Ge channel MOSFETs with NiGe metal S/D and FUSI gate, which are simultaneously formed by germanidation and silicidation, respectively. This combination of the NiGe metal S/D structure and the NiSi FUSI/SiO_2 gate stack allows us to realize the significant performance enhancement through superior Ge MOS interface properties, low thermal budget and the appropriate control of V_{th}.

Concept of NiGe metal source/drain MOSFET

NiGe metal source/drain

As shown in Fig 1, the measured sheet resistance of NiGe is found to have quite low values of 6 Ω/sq. or less at x_j=30nm, which is confirmed by simulations. Fig. 2 shows the typical NiGe/ Ge Schottky diode characteristics. The fine rectifying (ϕ_{bn}～ 0.6eV) and almost ohmic (ϕ_{bp}～0.06eV) characteristics are achieved for n-Ge and p-Ge substrates, respectively. The Fermi level pinning around the valence band edge at NiGe/Ge interfaces [2] is suitable for the application to pMOSFETs, because of the high drive current and low off current characteristics. The thermal stability of these Schottky diodes is also confirmed in Fig 3. Below 400 °C, n values of the diodes are kept almost unchanged. The gate length dependence of the total resistance of TaN gated MSD MOSFETs and conventional pn junction SD MOSFETs are compared in Fig.4. The parasitic resistance of the MSD MOSFET is found to be reduced down to 31 % of the value in the conventional pn junction.

NiSi FUSI gate

To maintain the high mobility characteristics and the proper V_{th} control, we adopt the combination of SiO_2 gate insulator with nickel silicide FUSI gate, because SiO_2/Ge interfaces are expected to yield the high mobility characteristics under the superior interface properties [5, 6]. It is known, furthermore, that the Fermi level of non-doped NiSi locates close to the valence band edge of Ge and the dopant segregation technique can also control V_{th} [7], as shown in Fig 5. Fig. 6 shows that there exists a process temperature window to simultaneously realize both the S/D formation and the gate silicidation. As a result, the NiGe S/D with an appropriate junction depth and the NiSi FUSI gate can be fabricated simultaneously by controlling the Ni/Si ratio depending on the Si gate height.

MOSFET fabrication

Nickel germanide metal S/D pMOSFETs were fabricated on n-type (Sb dope) (100) Ge substrates with a resistivity of 0.1-0.3Ωcm. The fabrication process flow is summarized in Fig. 7. As the gate insulator, 10nm SiO_2 was deposited by LPCVD at 420°C and a-Si was deposited at 525°C successively. After the gate and spacer formation, self-aligned germanidation (for S/D) and silicidation (for gate) processes were carried out by Ni sputtering and RTA at 400°C. Throughout these processes, the temperature was kept below 525°C.

Device characteristics

Fig. 8 shows the XSEM and XTEM micrographs of a NiSi metal gate NiGe S/D MOSFET. HRTEM and EDX results reveal that the interface is smooth and the FUSI gate is composed of NiSi. A C-V curve of the NiSi/SiO_2/n-Ge gate stack and the I_d-V_g characteristics of L_g=120μm devices are shown in Fig 9 and Fig.10, respectively. The good device characteristics are demonstrated. The experimental threshold voltage of -0.05V is in good agreement with the value expected from the combination of the FUSI NiSi gate work function and p-type Ge channels, suggesting that there is no significant V_{th} shift due to fixed charges or interface charges. The interface state extracted from the S factor is 8.7×10^{11} $cm^{-2}eV^{-1}$.

Fig. 11 and 12 show the current in the linear region and the transconductance characteristics, respectively, of FUSI NiSi metal gate NiGe S/D Ge MOSFETs and Al gate pn junction S/D Ge MOSFETs with the same gate oxides. Almost 7 time higher performance enhancement in the NiGe S/D MOSFETs is observed in both the linear and the saturation regions, attributed to the reduced S/D series resistance. Fig. 13 shows the effective hole mobility extracted by the split C-V method. The mobility of FUSI NiSi metal gate NiGe S/D MOSFETs (440 cm^2/Vs at 0.1MV) is found to be 3.4 times higher than the Si hole universal mobility. This peak mobility is the highest one among the values in unstrained Ge pMOSFETs, reported so far [4].

Conclusion

We have successfully demonstrated the high mobility Ge channel metal S/D pMOSFETs with NiSi FUSI gate. The hole mobility was 3.4 times higher than the Si hole universal one. As a result, the combination of the Ni germanided metal S/D and the NiSi FUSI formed from a-Si films deposited at low temperatures is a promising integration scheme with low thermal budget.

Acknowledgements

The authors would like to thank Drs. M. Hirose, T. Kanayama, and T. Masuhara for their continuous supports. This work was supported by NEDO.

References

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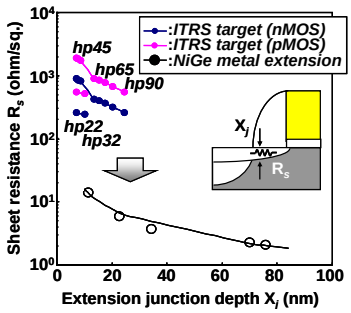

Fig.1.NiGe sheet resistance compared with the ITRS target of SDE sheet resistance.

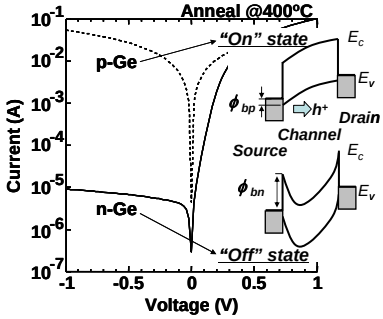

Fig. 2. Diode characteristics of NiGe/Ge junction. Fine rectifying and almost ohmic characteristics were achieved for n-Ge and p-Ge substrates, respectively.

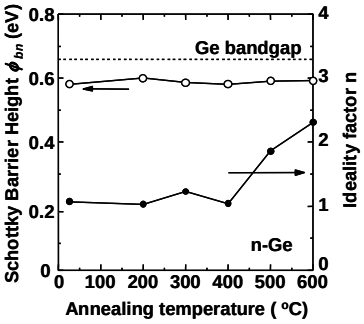

Fig.3. Thermal stability of NiGe / Ge diodes. Below 400ºC, the n values were kept almost identical.

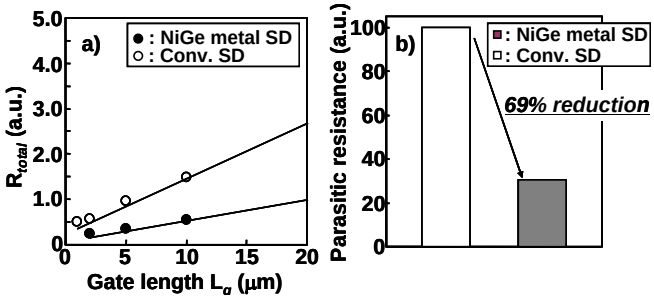

Fig.4. (a) Gate length dependence of total resistance of TaN gated MSD MOSFETs and conventional pn junction SD MOSFETs. (b) The parasitic resistance of MSD MOSFET is reduced to 31 % of the conventional SD case.

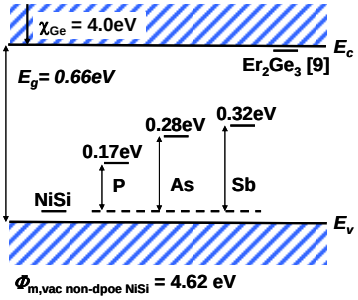

Fig.5. Work function range of NiSi with and w/o doping and the other metal gate materials for Ge channel MOSFETs.

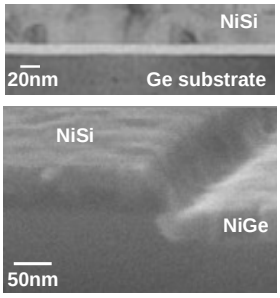

Fig.8.XTEM and XSEM of a NiGe S/D Ge pMOSFET with NiSi gate.

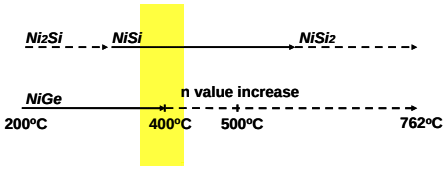

Fig.6. Process temperature window where S/D formation and gate silicidation become compatible.

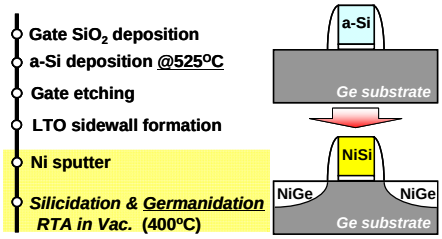

Fig.7. Fabrication process flow.

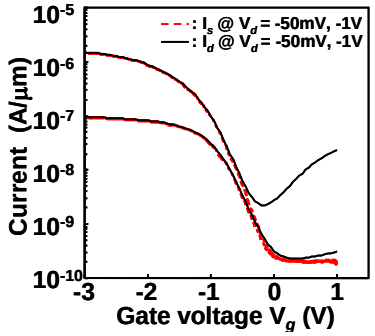

Fig.10. I_d, I_s -V_g characteristics of a L_g=120μm device.

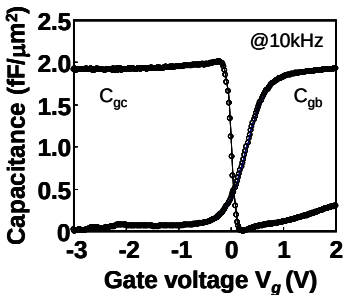

Fig.9. Split C-V curves of NiSi/SiO_2/n-Ge gate stack.

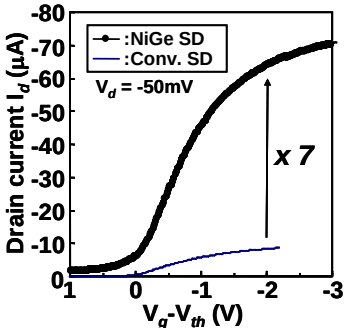

Fig.11. Linear I_d curve of L_g=80μm device.

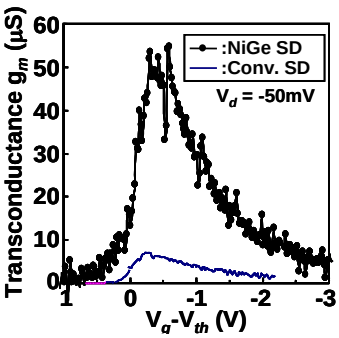

Fig.12. Transconductance curve of L_g=80μm device.

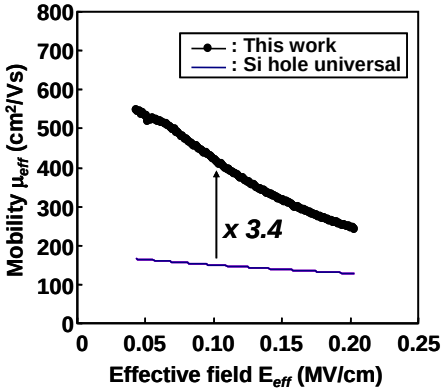

Fig.13. Effective mobility of FUSI NiSi metal gate NiGe S/D MOSFET (440 cm^2/Vs at 0.1MV) was 3.4 times higher than Si hole universal one.