B-1-2

Integration of Dual Channels MOSFET on Defect-Free, Tensile-Strained Germanium on Silicon

H. Zang[1,2], W. Y. Loh[2], J. D. Ye[2], T. H. Loh[2], G. Q. Lo[2], Byung Jin Cho[1*]
[1]Silicon Nano Device Lab, Dept of ECE, National University of Singapore, 117576 Singapore, *email: elebjcho@nus.edu.sg
[2]Institute of Microelectronics, 11 Science Park Road, 117685 Singapore

Abstract - We report on a novel Ge CMOSFET with ultra-thin (EOT~14 Å) HfO_2/TaN gate stack on p-type Si substrate without using graded SiGe buffer layer. High quality tensile-strained Ge channel (279 nm) is grown directly on Si wafer using a novel heteroepitaxial growth technique at temperature 350ºC-600ºC. Drain currents of 20μA/μm for p-MOS and 10μA/μm for n-MOS at $|V_g-V_T|$=1.2V were achieved for L_g = 5μm with low gate leakage of 10^{-4}~10^{-5}A/cm^2 at 1V. Peak hole mobility (measured by split C-V) for the epi-Ge channel is 250cm^2/Vs, which is more than 2× higher than universal hole mobility in Si. Ge layer is grown under ultrahigh vacuum chemical-vapor-deposition (UHVCVD) and is characterized by atomic forces microscopy, Micro-Raman and TEM with root-mean-square surface roughness (0.425nm), etch pit density of ~6×10^6 cm^{-2} and tensile-strain of up to ~0.67%. ***Monolithic integration of tensile-strained Ge CMOSFET on Si wafer is demonstrated, for the first time.***

1. INTRODUCTION

Ge MOSFETs have attracted much attention for future high-performance CMOS devices due to its high carrier mobility (electron ~3×; hole ~4×) as compared to Si. Although Ge CMOSFET have been reported previously on bulk Ge wafer [1-3], integration on Si wafer is hindered by the 4% lattice mismatch between Si and Ge. As a result, high density defects in Ge epi-layer and poor surface roughness due to island growth are typically observed [4]. To avoid strain relaxation and dislocations, thin super lattice (SL) Ge (<5nm) on Si has been reported previously [5, 6] but the resultant compressive strain in Ge is detrimental for n-MOSFET. Surface-smooth Ge epitaxial layer can be grown directly on Si wafer using multi-step hydrogen annealing [7], surfactant mediated growth [8] and two-step growth method [9-11]. Key advantage of the two-step growth approach is the tensile strain induced in Ge with ε = 0.2% [9, 10]. Nevertheless, the two-step epi-grown Ge layer still suffers from high threading-dislocation density (~9.5×10^8cm^{-2}). In this work, we demonstrate p-MOS and n-MOS on tensile-strained Si and Ge (s-Si/s-Ge) with HfO_2/TaN gate. Two-step growth of Ge layer (3000A) with low threading dislocation (6×10^6cm^{-2}) is realized on Si substrate, without cyclic annealing step, by UHVCVD with an intermediate ultrathin SiGe buffer [11] and compliant Si epi layer.

2. DEVICE FABRICATION

Devices were fabricated using standard CMOS process flow on 8" p-type Si (100). Ultrathin Si (10nm), $Si_{0.8}Ge_{0.2}$ (350-400˚C) buffer of thickness ~25nm, and strain-relaxed Ge was sequentially deposited in a UHV epi-chamber. For the two-step Ge process, a low temperature (400˚C) LT-Ge seed was first grown followed by high temperature HT-Ge (279nm thick) growth at 550-600˚C[9,10] and capped with 3nm tensile s-Si for CMOS optimization [5]. P- and N-well were formed with B/4×10^{12}cm^{-2}/60KeV and P/4×10^{12}cm^{-2}/110KeV implants and activated at 600˚C. After standard cleaning process, 6nm HfO_2 was deposited by PVD sputtering and annealed in O_2 ambient. Transistors with gate length of L_g = 0.5 to 10 μm were fabricated. **Fig. 1** shows the schematic of fabricated CMOS transistors.

3. RESULTS AND DISCUSSION

Figure 2 shows the high resolution TEM of Si/SiGe/Ge hetero-structure. Misfit/slip dislocations of a/2<110> 60º types are mainly confined within the 25nm SiGe buffer layer and at the SiGe/Ge interface and do not permeate across the entire Ge layer. As a result, the Ge layer above Ge/SiGe interface is almost *defect-free*. AFM measurement on Ge epitaxy (10μm×10μm) shows surface RMS of 0.425nm (**Fig. 3**). **Fig. 4** shows that Raman spectrum of the Ge film grown on Si. The Ge–Ge LO phonon peaks at 298.3 cm^{-1} as compared to 301.1 cm^{-1} for bulk Ge. From the Raman peak shift for Ge on Si, an in-plane strain $\varepsilon_{\|}$ can be calculated from the relationship [12] $\Delta\omega_{strain}=(1/\omega_0)*[q-(C_{12}/C_{11})p]\varepsilon_{\|}=B\varepsilon_{\|}$ where C_{11}, C_{12} are alloy elastic constants and q and p are the strain tensor constants. Using parameters from [12], B = -415 cm^{-1} with strain $\varepsilon_{\|}$ = 0.67% are obtained. Tensile strain is induced in Ge due to the lower thermal coefficient of Si compared to Ge, which tends to suppress the Ge lattice shrinkage during cooling. Our results are better than that in [9, 10] and may be attributed to the additional SiGe/Si compliant layer which allow full relaxation of the Ge during HT-growth.

Fig. 5 shows the CV characteristics of Ge p-MOSFET. The EOT of HfO_2 is 1.4 nm. The Si cap and the strong valence band offset of the strained Si/Ge heterostructure are responsible for capacitance loss in p-MOS inversion region [5]. When $|V_g|$ is high (V_g<-1.5V), the holes which are confined in the Ge layer, repopulate the s-Si layer, resulting in capacitance recovery. Due to epi-Si passivation, the leakage current of HfO_2 is reduced to 10^{-4} ~10^{-5}A/cm^2 (EOT=1.4nm) at $|V_g|$ = 1V, which is comparable with the published HfO_2 on Si results [13, 14] and about 2 orders lower than the published HfO_2 on Ge results [1, 2]. **Fig. 6-11** illustrate the device characteristics of the Ge CMOSFETs. **Figs. 9 and 10** show the I_d-V_g plots for the p- and n-MOSFETs. The off-state leakage current is in the order of 10^{-2} μA/μm for p-MOS and 10^{-3} μA/μm for n-MOS ($|V_d|$=0.05V). Under high V_d, gate induced drain leakage current (GIDL) is significant due to the narrow Ge band-gap, resulting in higher carrier band-to-band tunneling [15]. The inserts in **Figs. 8 and 9** show the transconductance (g_m) at V_d = ±50mV for n- and p-MOSFET. **Fig. 10** shows the channel mobility for Ge p-MOSFET. The Ge channel shows higher hole mobility with up to 100% (2×) enhancement compared to Si universal hole mobility. **Table-1** benchmarks the device parameters for Ge p-MOSFET on Ge bulk and on Si (including our work). Tensile-strained Ge on Si shows a better hole mobility compared to Ge bulk but is inferior to ultra-thin Ge on Si superlattice. This is however mitigated by the improved leakage and much simpler integration scheme of dual channel n-/p-MOSFETs on Si/SiGe/Ge hetero-structure.

4. CONCLUSION

High quality tensile-strained ($\varepsilon_{\|}$ = 0.67%) Ge epi-layer on Si wafer is achieved by two-step Ge growth method using an intermediate SiGe buffer and Si compliant layer. Ge CMOSFETs are successfully demonstrated based on this technique with 2× hole mobility improvement over Si universal mobility and leakage of 10^{-4} ~ 10^{-5} at 1V.

REFERENCES: [1] N.Wu *et al*; *EDL.*, **25,** 631 (2004). [2] Q.C.Zhang *et al, ISDRS*, 256, (2003). [3] N.Wu *et al*; *EDL,* **27** 479 (2006) [4] G. Masini *et al, EDL*, **48,** 1092 (2001) [5] O. Weber *et al*; *IEDM Tech. Dig.*, 137, (2005) [6] A. Ritenour *et al, IEDM Tech. Dig.*, 433 (2003) [7] A. Nayfeh *et al*; *EDL*, **26** 311 (2005) [8] T. Schmidt, *APL.*, 74(10), 1391 (1991) [9] Y. Ishikawa *et al.*, *APL*, 82(13), 2044 (2003) [10] J.F. Liu *et al*; *APL.*, **87**, 011110 (2005) [11] T.H. Loh et al, *APL.* **90**, 092108 (2007) [12]J. Zi *et al*., Prog. Surf. Sci., 54(1), 69 (1997) [13] W. Tsai *et al*, *VLSI Tech. Symp.* 3A-3, (2003) [14] H.Y. Yu et al, *IEDM*, p.99 (2003) [15] T. Krishnamohan *et al.,* VLSI, 82, (2005).

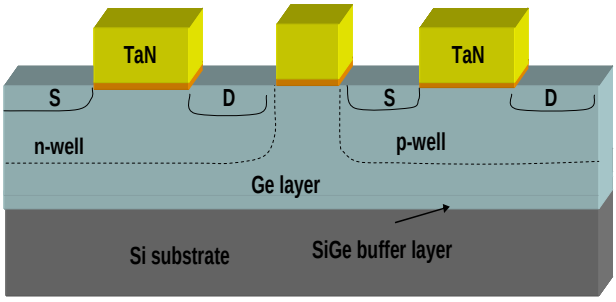

Fig. 1 Schematic diagram of the Ge MOSFET fabricated on Si wafer. Gate stack consists of 6nm HfO_2/TaN (100nm).

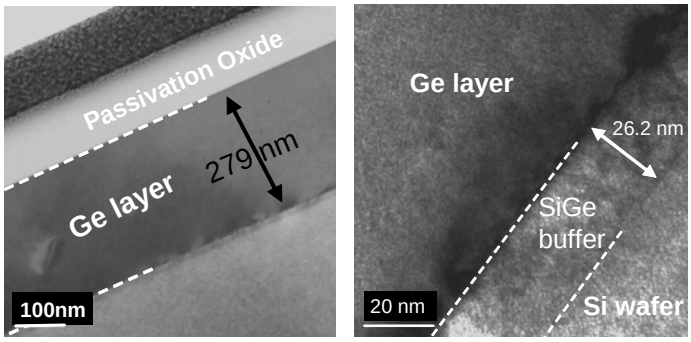

Fig. 2 HR-TEM images of the heterostructure epitaxial layers of Si/SiGe/Ge layers. Misfit dislocations are confined within the SiGe buffer and at the interface of SiGe/Ge .

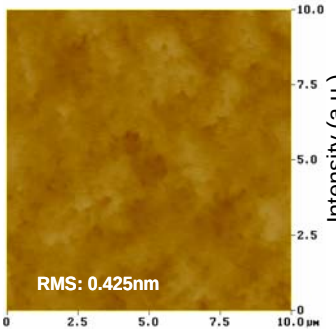

Fig. 3 AFM of grown Ge surface on 10μm × 10μm pad. Ge surface shows very good surface roughness of RMS of 4.25Å

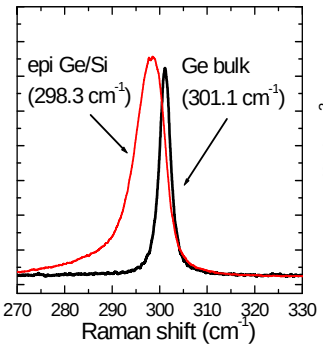

Fig. 4 Raman Spectra for epi-Ge on Si wafer and Ge bulk. Phonon peak for Ge on Si downshift, indicating tensile strain in Ge. Spectra broadening for Ge on Si is due to Ge intermixing with Si cap.

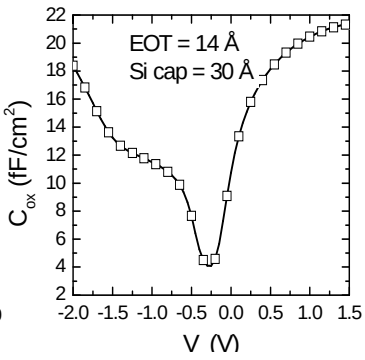

Fig. 5 C-V characteristics for Ge p-MOSFET. HfO_2(6nm) /TaN on Si/Ge shows accumulation EOT of 14 Å.

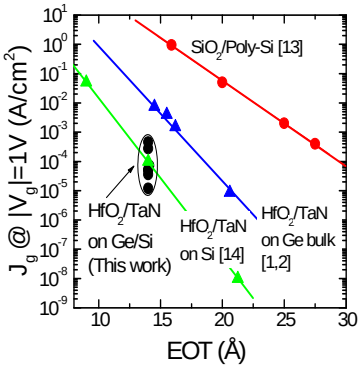

Fig. 6 High-k gate dielectric leakage current@ $|V_g|$=1V as function of EOT. J_g is comparable to [14] on Si substrate but better than those on Ge bulk [1,2]

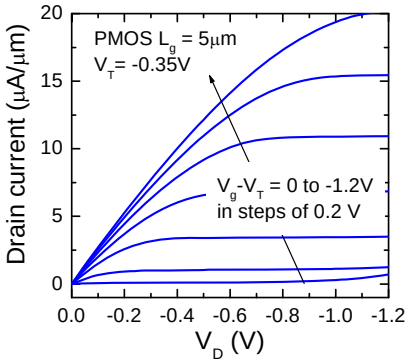

Fig. 7 I_d-V_d characteristics for tensile strained Ge p-MOSFET.

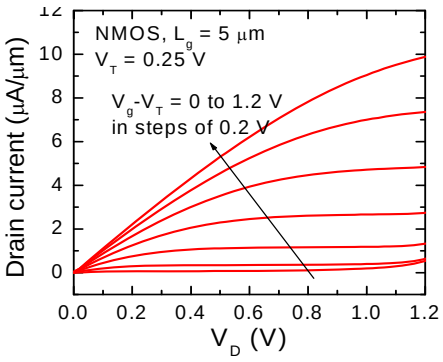

Fig. 8 I_d-V_d characteristics for s-Si/Ge n-MOSFET on n-Si bulk.

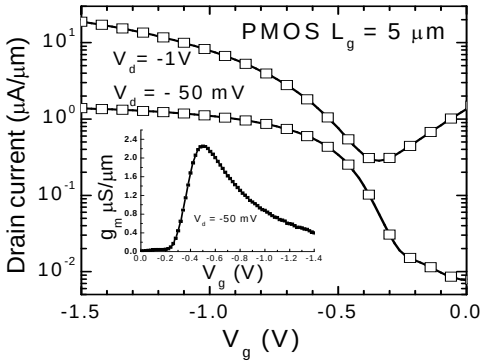

Fig. 9 I_d-V_g characteristics for Ge p-MOSFET. The insert shows corresponding g_m for V_{DS} = - 50 mV. High off state leakage is due to lack of halo implant

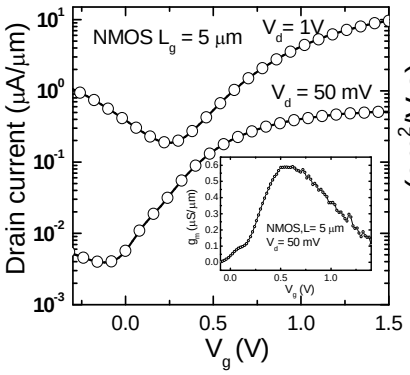

Fig. 10 I_d-V_g characteristics for strained Si/Ge channel n-MOSFET. The insert shows the g_m for V_{DS} = 50 mV.

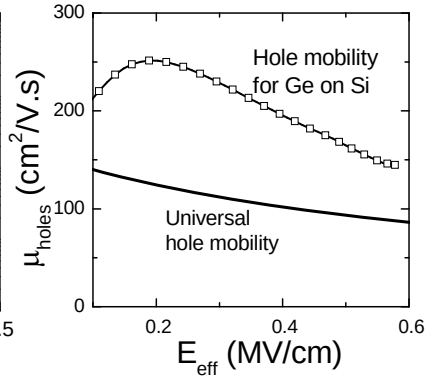

Fig. 11 Hole mobility for Ge p-MOSFET measured using split CV method. 2X hole mobility improvement is achieved as compared to Si universal mobility. .

Transistor structure	L_g (μm)	EOT (Å)	J_g@ Vg=1V (A/cm^2)	μ_{hole} @ 0.2 MV/cm (cm^2/V-s)
Ge bulk p-MOS with HfON dielectric [1]	20	20.6	10^{-5}-10^{-6}	130
Ge on Si p-MOS with GeON/Si O_2 [2]	6	140	N.A.	95
s-Ge on r-SiGe buffer with HfO_2 [5]	≤ 0.2	14	10^{-3}	≥ 490
Bulk Ge / s-Ge on Si with HfO_2 [6]	3	16	10^{-7}-10^{-6}	135/160
s-Ge on Si p-MOS with HfO_2 (This work)	**0.5**	**14**	**10^{-4}-10^{-5}**	**250**

Table. 1 Summary of Ge p-MOSFET performance with different hetero-structures and bulk substrate. Current results shows good hole mobility with reasonable gate leakage in Ge p-MOS on Si substrate.