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Electrical Stress Effects on Mobility of Germanium-On-Insulator (GeOI) pMOSFETs with HfO_2 Gate Dielectric

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1. Introduction

In order to achieve high device performance required in nano-scale MOSFETs, lots of research efforts have been concentrated on channel engineering and high-*k* gate dielectric materials. Several types of germanium (Ge)-based devices have been proposed [1-6] to utilize high mobility of carriers in Ge material due to smaller effective masses of electrons and holes compared with those in silicon (Si) material. However, most of the Ge MOSFETs reported have adopt buried channel with thin Si cap layer on top of Ge channel to obtain stable oxide gate dielectric. Although mobility enhancement has been reported in all the proposed buried channel Ge MOSFETs, a surface Ge-channel structure is strongly desirable to achieve the highest gate capacitance. Although the recent successful development of high-*k*/Ge pMOSFETs [1]-[3] have demonstrated high device performance, there are few report on mobility degradation of Ge devices due to charge trapping/de-trapping effects, which is also one of crucial reliability issues for HfO_2 gate dielectric on Si MOSFETs [7].

In this work, by applying various electrical stresses of hot carrier (HC) injection and Fowler-Nordheim (FN) gate stress with different gate bias polarities, we have investigated the mobility characteristics of HfO_2/Ge pMOSFETs reported in [1].

2. Experimental and Results

A schematic cross section of HfO_2/SiGeOI pMOSFET used for this study is shown in Fig. 1. At first, in order to confirm the device characteristics, we have measured dc-characteristics of fresh devices. Fig. 2(a) and (b) show the measured typical current components (I_d, I_s, and I_g) and gate to channel capacitance (C_{gc}) characteristics with respect to gate voltage (V_g) and several back-side Si-substrate biases (V_{ck}), rspectively. As seen in Fig. 2(a), it is found that the gate leakage (I_g) through HfO_2 dielectric (~6.5 nm) reveals ~0.1 nA/μm at V_g= −3 V, which is as low as 10^4× compared to the drain (I_d) and source (I_s) currents. Also, from Fig. 2(b), it is found that I_d and C_{gc} characteristics have a strong V_{ck} dependence due to the threshold voltage shift. In this study, all measurement for I_d–V_g and C_{gc}–V_g have been carried out at V_{ck}=5 V because the obtained C_{gc} (plateau region in Fig. 2(b)) in our case show unstable even the V_{ck} is biased 0 V. We believe that this phenomena is caused by the floating Ge body.

Next, before and after HC stress (V_g=V_d= -1V, $\Delta t=10^3$ s), device characteristics of GeOI pMOSFETs for W=100 μm L=2 μm have been measured (Fig. 3(a), (b), and (c)). After HC stresss, results are monitored for both the case of exchanging S/D electrodes (r-mode) and without exchanging (f-mode) and compared with fresh ones. It is found that all the device performance of I_{ON}, G_m, and hole mobility (μ_h) after HC stress show consistent degradation under the r-mode measurement, which is similar to the widely reported reliability issues in Si-channel devices.

To understand the effects of trapped charges at interface traps or inside traps in gate dielectric on mobility, we also carried out FN stress. To minimize gate overlap effect from S/D region, we have selected longer channel device as L=5 μm compared with ones used in HC stress. Here, we have compared gate-bias polarity dependence [9] by applying two different sequences of negative gate biased FN stress following positive stress (NFN→PFN) and positive gate stress first (PFN→NFN), as shown in Fig. 4(a)-(c) and Fig. 4(d), respectively. The most important finding of this study is that device degradation for Ge pMOSFETs occurrs mainly after positive gate-bias FN stress. As seen in Fig. 4(d) and (e), the recovery of device performance similar to NBTI (PBTI) results in Si devices have been also observed in Ge-channel devices in our case.

3. Conclusion

With HfO_2/Ge-pMOSFETs device degradation under electrical stresses was investigated. According to the results of HC and FN stress, it seems that mobility degradation in HfO_2/Ge-pMOSFETs are easily affected by the trapped charges in gate dielectric layer.

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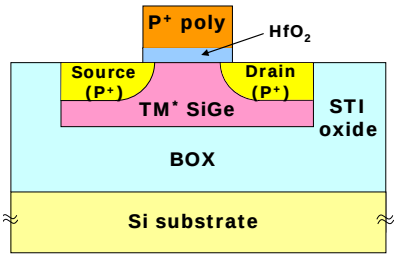


Fig. 1. Schematic cross section of GeOI PMOSFET with on silicon germanium (SiGe) channel by the thermal mixing (TM) technique [1] on buried oxide (BOX) and HfO_2 gate dielectric.

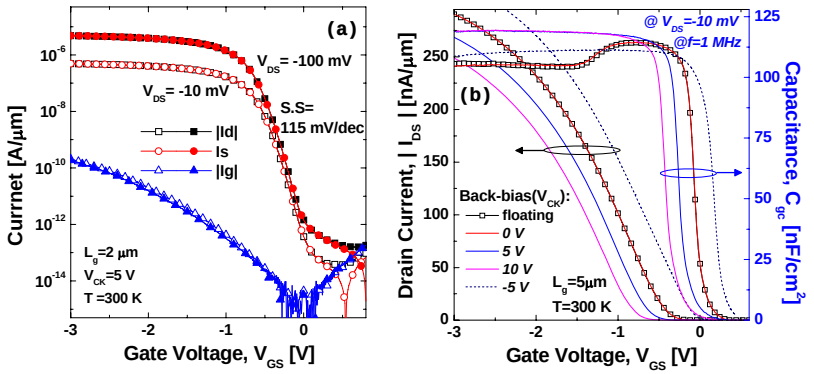


Fig. 2. (a) Measured typical current characteristics of HfO_2/GeOI pMOSFET (L=2 μm) with respect to gate voltage for Vds= –10 mV and –100 mV, respectively. (b) Drain current (Id @Vds= –10 mV) and inversion capacitance (Cgc @f =1 MHz) are shown as a function of gate voltage with variables of back-bias (Vck) for L=5 μm. The measured Cgc shows unstable even biased with Vck=0 V.

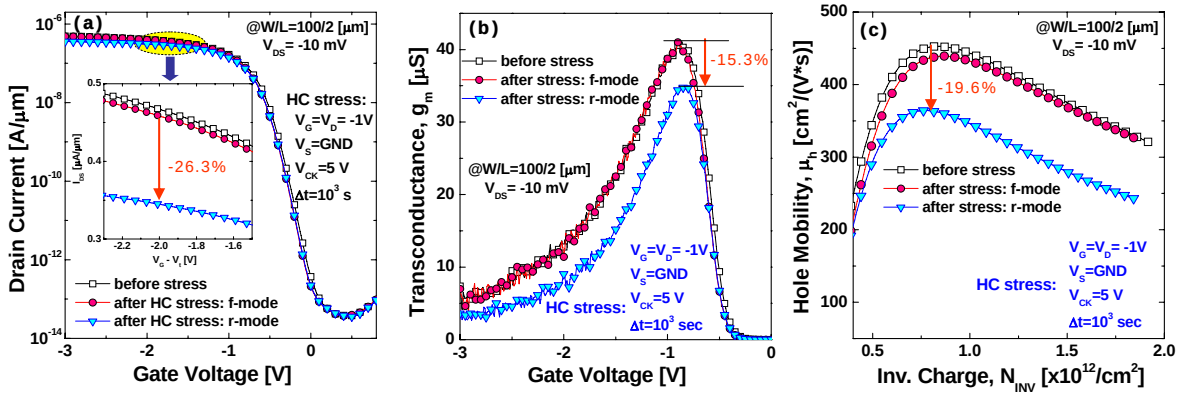
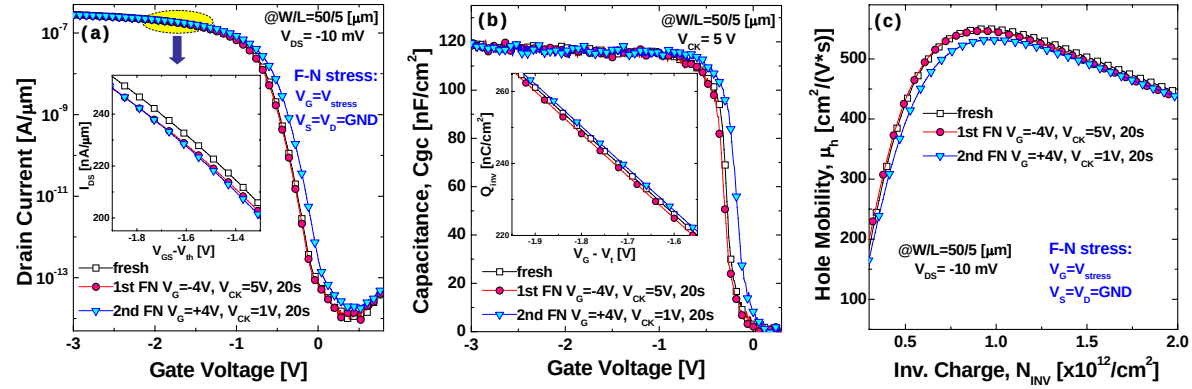


Fig. 3. Hot carrier stress (@Vg=Vd= –1V, Δt=1 ks) effects on device performance of HfO_2/GeOI pMOSFETs. After stressing, (a) Id-Vg (linear scale in inset), (b) transconductance (gm), and (c) extracted hole mobility, respectively, are compared with before stressed ones all for Vds= –10 mV by r-mode (exchanging source and drain electrodes after stress) and f-mode (the same configuration for source and drain electrodes before and after HC stress) measurement.



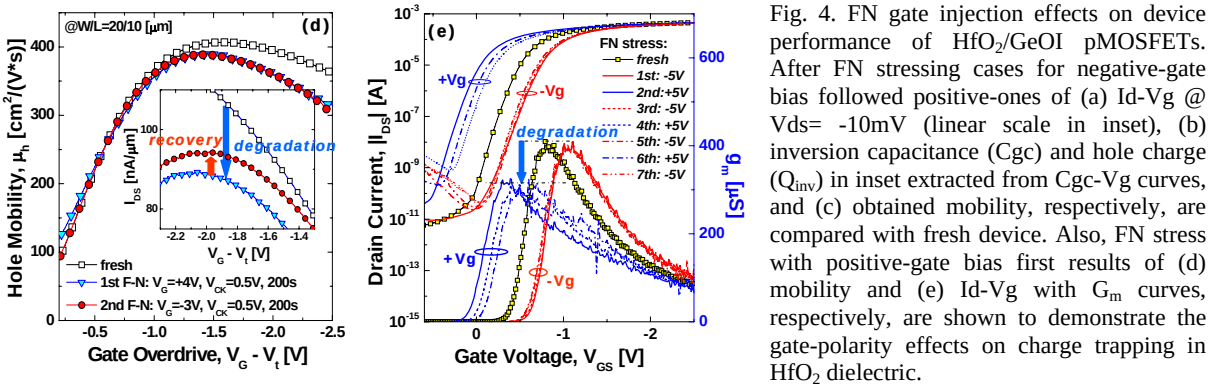


Fig. 4. FN gate injection effects on device performance of HfO_2/GeOI pMOSFETs. After FN stressing cases for negative-gate bias followed positive-ones of (a) Id-Vg @ Vds= -10mV (linear scale in inset), (b) inversion capacitance (Cgc) and hole charge (Q_{inv}) in inset extracted from Cgc-Vg curves, and (c) obtained mobility, respectively, are compared with fresh device. Also, FN stress with positive-gate bias first results of (d) mobility and (e) Id-Vg with G_m curves, respectively, are shown to demonstrate the gate-polarity effects on charge trapping in HfO_2 dielectric.