Silicon Strain-Transfer-Layer (STL) and Graded Source/Drain Stressors for Enhancing the Performance of Silicon-Germanium Channel P-MOSFETs

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ABSTRACT

A novel strained Si$_{0.60}$Ge$_{0.40}$ channel p-FET that employs an embedded silicon strain-Transfer-Layer (STL) is demonstrated for the first time. The silicon strain-transfer-layer strengthens the coupling of lattice interactions between the lattice-mismatched source-drain (S/D) stressors and the channel region, and induces uniaxial compression in the SiGe channel. Devices with gate length $L_G$ down to 50 nm were fabricated. The strain effects result in 84% drive current improvement over unstrained Si channel devices. Carrier backscattering study was performed to illustrate carrier transport characteristics of the strained transistors.

INTRODUCTION

New device architectures and channel materials would be required for realizing high performance levels in nanoscale MOSFETs. In addition, strain engineering can be exploited to enhance the mobility even further. p-FETs with SiGe and Ge channel regions have enhanced mobility and performance over Si-channel p-FETs [1]. Further strain enhancement techniques can be applied on SiGe channel p-FETs to achieve higher levels of performance.

In this paper, we report the first demonstration of a novel strained SiGe channel p-FET that employs a SOI layer beneath the SiGe channel as a Strain-Transfer-Layer (STL). The SOI layer not only serves to induce a biaxial compressive strain in the SiGe channel, but also improves the lattice interaction between S/D stressors and the channel region for enhanced drive current. A complementary approach has been reported for p-FETs with an embedded SiGe strain-transfer-structure (STS) [2], but the pseudomorphically grown STS is constrained by the underlying substrate and therefore lacks compliance. The Si STL employed in this work could be compliant and would be a highly effective strain-transfer-structure.

DEVICE FABRICATION

Fig. 1 illustrates the cross-sections of device structures fabricated in this work, including: (a) unstrained control SOI p-FET, (b) Uniaxially strained SOI p-FET with recessed $Si_{0.75}Ge_{0.25}$ S/D, (c) strained-SiGe/Si-PLL STL p-FET with raised and un recessed $Si_{0.75}Ge_{0.25}$ S/D, (d) strained-SiGe/Si-STL p-FET with raised and recessed $Si_{0.75}Ge_{0.25}$ S/D, and (e) strained-SiGe/Si-STL p-FET with recessed and graded $Si_{0.80}Ge_{0.20}$ S/D regions. Grading of $Si_{0.80}Ge_{0.20}$ S/D aimed to minimize misfit dislocation nucleation and propagation due to the large lattice mismatch between the Si STL and the S/D. Fig. 2 shows the transistor fabrication process. SOI substrates were used as the starting material. Nano-beam diffraction measurements confirmed that the starting substrate was relatively unstrained. Following active area definition, epitaxial growth of a 15 nm strained $Si_{0.75}Ge_{0.25}$ was performed on three SOI wafers in a UHV-CVD system. Threshold voltage adjustment implants were then performed. This was followed by rapid thermal oxidation to form 2.5 nm gate dielectric, polysilicon gate deposition, and patterning. Devices with gate lengths $L_G$ down to 50 nm were fabricated. S/D extension and halo implants were performed. 20 nm spacers were formed. The S/D regions of Devices (b), (d) and (e) [refer to Fig. 1] were recessed by 25 nm, while Devices (a) and (c) did not undergo a recess etch. Selective epitaxial growth of Si was performed on Devices (a) and (b) while $Si_{0.75}Ge_{0.25}$ growth was performed on Devices (c) and (d). A graded $Si_{0.80}Ge_{0.20}$ growth was performed on Device (e) by growing 2 nm $Si_{0.75}Ge_{0.25}$ followed by 2 nm $Si_{0.80}Ge_{0.20}$. Cycles of $Si_{0.80}Ge_{0.20}$ growth then followed. S/D implantation and dopant activation (RTA at 900°C, 60 sec) followed. All wafers underwent the standard BEOL steps. A typical transistor with tensile ESL is featured in the top cross-section of Fig. 3(a).

DEVICE CONCEPT

The Si layer beneath the $Si_{0.75}Ge_{0.25}$ channel induces biaxial compressive strain in the $Si_{0.75}Ge_{0.25}$ layer. The lattice mismatch between $Si_{0.75}Ge_{0.25}$ and Si is ~1.6%. The larger lattice constant of SiGe pulls the Si vertically at the hetero-junction and induces large uniaxial compressive strain to the $Si_{0.75}Ge_{0.25}$ channel [Fig. 3(b)]. Due to the compliant nature of the SOI, Si STL adds to the compressive stress originally present after channel epitaxy. The effectiveness of the Si STL is supported by stress simulation using Synopsys-SIE FLOOPS. Stress simulations show that the coupling between the Si STL and the $Si_{0.75}Ge_{0.25}$ S/D results in about ~1.97 GPa compressive stress in Device(e) [Fig. 3(d)], while it is ~0.62 GPa stress in the absence of Si STL. Device (f) [Fig. 3(c)].

RESULTS AND DISCUSSION

The Ge profile in the graded embedded-SiGe (p-SiGe) source/drain region is shown in Fig. 4. The Ge profile was determined by Auger Electron Spectroscopy (AES). The peak Ge concentration is controlled to be close to the channel to maximize strain effects. Fig. 5 compares the Si- and Ge-based devices. Incorporation of $Si_{0.75}Ge_{0.25}$ as the channel material gives 30% $I_{DSS}$ enhancement over the unstrained Si p-FET. With recessing the S/D regions to make use of the effect of the STS, the $I_{DSS}$ is further enhanced by 13%. Increasing the STL/S/D lattice mismatch significantly enhanced the drive current by a further 54%. It is clear that the interaction between the recessed SiGe S/D and the Si STL at the heterojunction enhances the channel strain. The $I_{DSS}$ characteristics are shown in Fig. 7.

The transconductance $g_m$ of Device(e) (Fig. 8) is ~104% higher than that of Device (c) ($Si_{0.75}Ge_{0.25}$ channel, un recessed S/D), and ~80% higher than that of Device (d) ($Si_{0.80}Ge_{0.20}$ channel, recessed S/D). The large improvement seen in Device (e) indicates mobility enhancement contributed by the interaction between the Si STL and the graded SiGe S/D with substantial lattice mismatch. The incorporation of Si STL provides significant improvement in p-FET $I_{DSS}$ (Fig. 9) at a fixed off-state current (~52% @ $I_{OFF}$ = 10 nA/µm). Fig. 10 plots the saturation drain current of various devices for different $L_G$. The progressively larger enhancement observed with reducing channel length points to increasing strain effects and consequential performance benefits with device scaling. Fig. 11 examines the dependency between the enhancement of near-equilibrium carrier mobility and the enhancement of $I_{DSS}$. Device (e) shows higher enhancement with uniaxial compressive strain than Device (d), as can be expected from the lattice mismatch of 0.6% and 0% respectively. Significant mobility enhancement of about 100% results in $I_{DSS}$ enhancement of about 50%. Fig. 12 plots the dependency of $I_{DSS}$ on active area width. In-plane compressive strain perpendicular to channel, degrades p-FET performance, and is particularly observed at large active areas.

Channel backscattering ratios of the p-FETs are also analyzed. Based on extracted $\lambda / \nu$ ratio [3], carrier backscattering ratio $\nu_{back}$ is calculated and plotted in Fig. 13. As $L_G$ shrinks, compressively strained p-FETs exhibits a larger $\nu_{back}$ at channel length smaller than 150 nm. This indicates when carriers are injected from source into channel, injected holes suffer more channel backscattering. Using measured $\nu_{back}$ and $I_{DSS}$, the carrier injection velocity is calculated and plotted in Fig. 14. For compressively strained p-FETs, slightly lower $\nu_{back}$ and much higher $\nu_{inj}$ are obtained, as observed in Fig. 14, which leads to a net gain in $I_{DSS}$. This suggests a stronger relationship between $\nu_{back}$ enhancement and $I_{DSS}$ gain. Substantial $\nu_{back}$ improvement in Device (e) can be attributed to dramatic reduction in $\nu_{inj}$. Fig. 15 summarizes the performance improvements achieved from the integration of the various combinations of Si STL and S/D combinations.

CONCLUSION

Lattice-mismatched and graded Si$_{0.60}$Ge$_{0.40}$ S/D was employed together with a Silicon Strain-Transfer-Layer for strain$_{0.75}Ge_{0.25}$ channel p-FETs. Considerable enhancement was achieved and is believed to be due to the lattice interaction between S/D stressors and the compliant Si STL, providing a platform for the integration of high-performance CMOS, where strained Si$_{0.75}Ge_{0.25}$ channel p-FETs can be integrated with strained n-FETs on the SOI layer.

REFERENCES

Unstrained Si channel + Si S/D observedLinLgradedL(e))

Fig. 1. Schematic depicting various strain schemes (a) unstrained Si, (b) recessed Si channel with SiGe S/D, and (c)strained Si channel with SiGe S/D.

Fig. 2. Process sequence showing key steps employed in strained transistors device fabrication. The integration of devices with Si STL and graded Si$_x$Ge$_{1-x}$ S/D facilitates studies of strain effects that modulate the strained SiGe channel for $I_{DS}$ enhancement.

Fig. 3. TEM picture of fabricated device. Device (a) showing the proximity of Si STL to the graded-Si$_x$Ge$_{1-x}$ S/D for enhanced interaction. Device (b) featuring channel strain modulation with Si STL. Micron-channel stressors of -50MPa and -100MPa, respectively, are observed.

Fig. 4. Auger Electron Spectroscopy depth profile of Ge content in the graded embedded Si$_x$Ge$_{1-x}$ S/D. Grading of S/D aimed to minimize misfit dislocation nucleation.

Fig. 5. Plot of $I_{DS}$ vs $V_{DS}$ for Devices (a) and (c). $I_{DS}$ enhancement of 30% is observed. Due to the higher hole mobility supported by the SiGe channel, drive current is enhanced.

Fig. 6. Plot of $I_{DS}$ vs $V_{DS}$ for Device (b). $I_{DS}$ enhancement of 15% is observed with $V_{GS}$ = -0.3V for the strained S/D device incorporated.

Fig. 7. Plot of $I_{DS}$ vs $V_{DS}$ for Devices (a), (b), and (c). Similar threshold characteristics were obtained for the devices, justifying comparison.

Fig. 8. Plot of $I_{DS}$ vs $V_{DS}$ for Devices (a), (b), and (c). $I_{DS}$ enhancement of 104% was observed in graded e-Si$_x$Ge$_{1-x}$ S/D (Device (e)) over unstrained Si$_x$Ge$_{1-x}$ S/D device.

Fig. 9. At $V_D$ of 100mV, a saturation drive current enhancement of 52% is achieved for Device (e) and 15% for Device (b) over unstrained Si$_x$Ge$_{1-x}$ S/D device.

Fig. 10. Plot of drive current as a function of $L_D$ for various schemes of strained devices with different stressors incorporated.

Fig. 11. Significant $I_{DS}$ enhancement observed in SiGe S/D device is attributed to the large gain in hole mobility and strain induced in channel.

Fig. 12. Narrower width results in relaxation of in-plane compressive strain parallel to channel direction and affects p-FET drive current.

Fig. 13. Impact of strain on extracted $r_m$ for various $L_D$. Higher $r_m$ is observed for strained devices. Despite more channel backscattering in strained devices, drive current was enhanced.

Fig. 14. Higher $r_m$ results in degradation of $R_m$. Much higher $r_m$ compensates $R_m$ reduction in strained devices, resulting in a net gain in drive current.

Fig. 15. Summary of device performance improvement, illustrating the effectiveness of Si STL in channel strain modulation.