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Silicon Strain-Transfer-Layer (STL) and Graded Source/Drain Stressors for Enhancing the Performance of Silicon-Germanium Channel P-MOSFETs

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ABSTRACT

A novel strained $Si_{0.75}Ge_{0.25}$ channel *p*-FET that employs an embedded silicon Strain-Transfer-Layer (STL) is demonstrated for the first time. The silicon strain-transfer-layer strengthens the coupling of lattice interactions between the lattice-mismatched source/drain (S/D) stressors and the channel region, and induces uniaxial compression in the SiGe channel. Devices with gate length L_G down to 50 nm were fabricated. The strain effects resulted in 84% drive current improvement over unstrained Si channel devices. Carrier backscattering study was performed to illustrate carrier transport characteristics of the strained transistors.

INTRODUCTION

New device architectures and channel materials would be required for realizing high performance levels in nanoscale MOSFETs. In addition, strain engineering can be exploited to enhance the mobility even further. *p*-FETs with SiGe and Ge channel regions have enhanced mobility and performance over Si-channel *p*-FETs [1]. Further strain enhancement techniques can be applied on SiGe channel *p*-FETs to achieve higher levels of performance.

In this paper, we report the first demonstration of a novel strained SiGe channel *p*-FET that employs a SOI layer beneath the SiGe channel as a Strain-Transfer-Layer (STL). The SOI layer not only serves to induce a biaxial compressive strain in the SiGe channel, but also improves the lattice interaction between S/D stressors and the channel region for enhanced drive current. A complementary approach has been reported for ***n***-FETs with an embedded SiGe strain-transfer-structure (STS) [2], but the pseudomorphically grown STS is constrained by the underlying substrate and therefore lacks compliance. The Si STL employed in this work could be compliant and would be a highly effective strain-transfer-structure.

DEVICE FABRICATION

Fig. 1 illustrates the cross-sections of device structures fabricated in this work, including: (a) unstrained control SOI *p*-FET, (b) Uniaxially strained SOI *p*-FET with recessed $Si_{0.75}Ge_{0.25}$ S/D, (c) strained-SiGe/Si-STL *p*-FET with raised and unrecessed $Si_{0.75}Ge_{0.25}$ S/D, (d) strained-SiGe/Si-STL *p*-FET with raised and recessed $Si_{0.75}Ge_{0.25}$ S/D, and (e) strained-SiGe/Si-STL *p*-FET with recessed and graded $Si_{0.60}Ge_{0.40}$ S/D regions. Grading of $Si_{0.60}Ge_{0.40}$ S/D aimed to minimize misfit dislocation nucleation and propagation due to the large lattice mismatch between the Si STL and the S/D. Fig. 2 shows the transistor fabrication process. SOI substrates were used as the starting material. Nano-beam diffraction measurements confirmed that the starting substrate was relatively unstrained. Following active area definition, epitaxial growth of a 15 nm strained $Si_{0.75}Ge_{0.25}$ was performed on three SOI wafers in a UHV-CVD system. Threshold voltage adjusts and well implants were then performed. This was followed by rapid thermal oxidation to form 2.5 nm gate dielectric, polysilicon gate deposition, and patterning. Devices with gate lengths L_G down to 50 nm were fabricated. S/D extension and halo implants were performed. 20 nm spacers were formed. The S/D regions of *Devices (b), (d)* and *(e)* [refer to Fig. 1] were recessed by 25 nm, while *Devices (a)* and *(c)* did not undergo a recess etch. Selective epitaxial growth of Si was performed on *Devices (a)* and *(b)* while $Si_{0.75}Ge_{0.25}$ growth was performed on *Devices (c)* and *(d)*. A graded $Si_{0.60}Ge_{0.40}$ growth was performed on *Devce (e)* by growing 2 nm $Si_{0.75}Ge_{0.25}$ followed by 2 nm $Si_{0.68}Ge_{0.32}$. Cycles of $Si_{0.60}Ge_{0.40}$ growth then followed. S/D implantation and dopant activation (RTA at 900°C, 60 sec) followed. All wafers underwent the standard BEOL steps. A typical transistor with tensile ESL is featured in the cross section TEM in Fig. 3(a).

DEVICE CONCEPT

The Si layer beneath the $Si_{0.75}Ge_{0.25}$ channel induces biaxial compressive strain in the $Si_{0.75}Ge_{0.25}$ layer. The lattice mismatch between $Si_{0.60}Ge_{0.40}$ and Si is ~1.6%. The larger lattice constant of SiGe pulls the Si vertically at the hetero-junction and induces a large uniaxial compressive strain to the $Si_{0.75}Ge_{0.25}$ channel [Fig. 3(b)]. Due to the compliant nature of the SOI, Si STL adds on the compressive stress originally present after channel epitaxy. The effectiveness of the Si STL is supported by stress simulation using Synopsys-ISE FLOOPS. Stress simulations show that the coupling between the Si STL and the $Si_{0.75}Ge_{0.25}$ S/D results in about -1.07 GPa compressive stress in *Device(d)* [Fig. 3(d)], while it is -0.62 GPa stress in the absence of Si STL, *Device (b)* [Fig. 3(c)].

RESULTS AND DISCUSSION

The Ge profile in the graded embedded-SiGe (***e***-SiGe) source/drain region is shown in Fig. 4. The Ge profile was determined by Auger Electron Spectroscopy (AES). The peak Ge concentration is controlled to be close to the channel to maximize strain effects. Fig. 5 compares the Si- and $Si_{0.75}Ge_{0.25}$- channel *p*-FETs. Incorporation of $Si_{0.75}Ge_{0.25}$ as the channel material gives 30% I_{Dsat} enhancement over the unstrained Si *p*-FET. With recess etching the S/D regions to make use of the effect of the Si-STL, the the I_{Dsat} is further enhanced by 13%. Increasing the STL-S/D lattice mismatch significantly enhanced the drive current by a further 54%. It is clear that the interaction between the recessed SiGe S/D and the Si STL at the heterojunction enhances the channel strain. The I_{DS}-V_{GS} characteristics are shown in Fig.7.

The transconductance G_m of *Device(e)* (Fig. 8) is ~104% higher than that of *Device (c)* ($Si_{0.75}Ge_{0.25}$ channel, unrecessed S/D), and ~80% higher than that of *Device (d)* [$Si_{0.75}Ge_{0.25}$ channel, recessed S/D]. The large improvement seen in *Device (e)* indicates mobility enhancement contributed by the interaction between the Si STL and the graded SiGe S/D with substantial lattice mismatch. The incorporation of Si STL provides significant improvement in *p*-FET I_{Dsat} (Fig. 9) at a fixed off-state current (~ 52% @ I_{off} = 100 nA/μm). Fig. 10 plots the saturation drain current of various devices for various L_G. The progressively larger enhancement observed with reducing channel length points to increasing strain effects and consequential performance benefits with device scaling. Fig. 11 examines the dependency between the enhancement of near-equilibrium carrier mobility and the enhancement of I_{Dsat}. *Device (e)* shows higher enhancement with uniaxial compressive strain than *Device (d),* as can be expected from the lattice mismatch of 0.6% and 0% respectively. Significant mobility enhancement of about 100% results in I_{Dsat} enhancement of about 50%. Fig. 12 plots the dependency of I_{Dsat} on active area width. In-plane compressive strain perpendicular to channel, degrades *p*-FET performance, and is particularly observed at large active areas.

Channel backscattering ratios of the *p*-FETs are also analyzed. Based on extracted λ_o/l_o ratio [3], carrier backscattering ratio $r_{sat\ t}$ is calculated and plotted in Fig. 13. As L_G shrinks, compressively strained *p*-FET exhibits a larger r_{sat} at channel length smaller than 150 nm. This indicates when carriers are injected from source into channel, injected holes suffer more channel backscattering. Using measured r_{sat} and I_{Dsat}, the carrier injection velocity is calculated and plotted in Fig. 14. For compressively strained *p*-FETs, slightly lower B_{sat} and much higher v_{inj} are obtained, as observed in Fig. 14, which leads to a net gain in I_{Dsat}. This suggests a stronger relationship between v_{inj} enhancement and I_{Dsat} gain. Substantial v_{inj} improvement in *Device (e)* can be attributed to dramatic reduction in λ_0 [3]. Fig. 15 summarizes the performance improvements achieved from the integration of the various combinations of Si STL and S/D combinations.

CONCLUSION

Lattice-mismatched and graded $Si_{0.60}Ge_{0.40}$ S/D was employed together with a silicon Strain-Transfer-Layer for strain engineering in $Si_{0.75}Ge_{0.25}$ channel ***p***-FETs. Considerable enhancement was achieved and is believed to be due to the lattice interaction between S/D stressors and the compliant Si STL. The Si STL serves as a platform for the integration of high-performance CMOS, where strained $Si_{0.75}Ge_{0.25}$ channel *p*-FETs can be integrated with strained *n*-FETs on the SOI layer.

REFERENCES

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[2] R. A. Donaton *et al,, IEDM Tech Dig*., pp.439, 2006.
[3] H. N. Lin *et al., Symp. on VLSI Tech Dig*., pp 174, 20

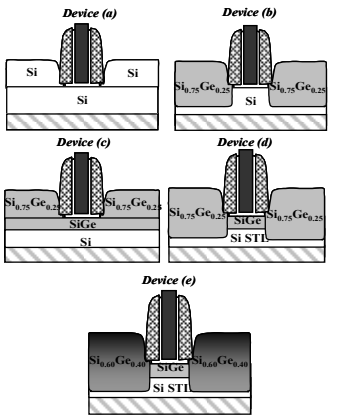

Fig. 1. Schematic depicting various strain schemes: ***(a)***Unstained Si, ***(b)*** Recessed Si channel with SiGe S/D, ***(c)*** Biaxial strained SiGe channel, ***(d)*** Recessed $Si_{0.75}Ge_{025}$ S/D coupled with Si STL, ***(e)*** Recessed graded ***e***-$Si_{0.6}Ge_{0.4}$ S/D coupled with Si STL

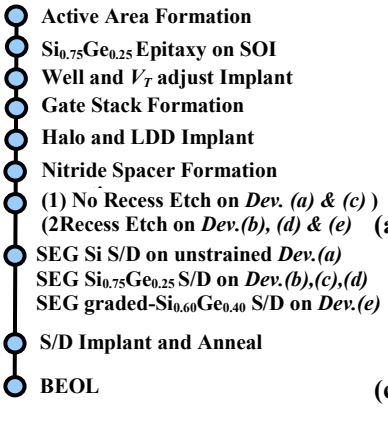

Fig. 2. Process sequence showing key steps employed in strained transistors device fabrication. The integration of devices with Si STL and graded $Si_{0.6}Ge_{0.4}$ S/D facilitates studies of strain effects that modulates the strained SiGe channel for I_{Dsat} enhancement.

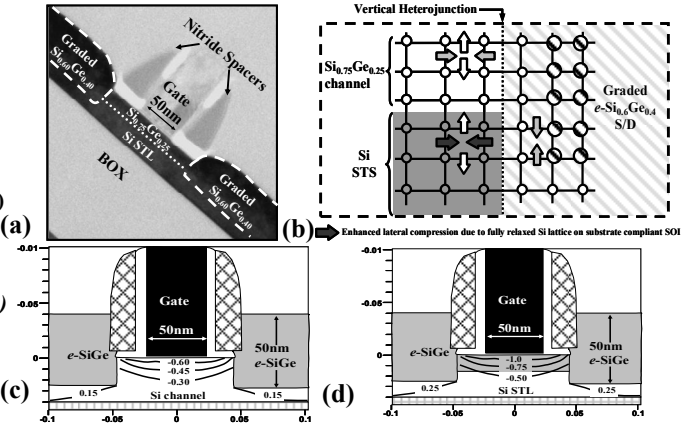

Fig. 3. (a) TEM picture of fabricated device,***Device (e)*** showing the proximity of Si STL to the graded-$Si_{0.6}Ge_{0.4}$ S/D for enhanced interaction, (b)Concept of the efficiency of stress-transfer layer in inducing additional compression in channel for enhanced performance is illustrated, (c) Simulated stress ε_{xx} (in GPa) contour plot for ***Device (b)*** recessed S/D, and (d) for ***Device(d)*** featuring channel strain modulation with Si STL. Mid-channel stresses of -620MPa, and -1070MPa, respectively are observed.

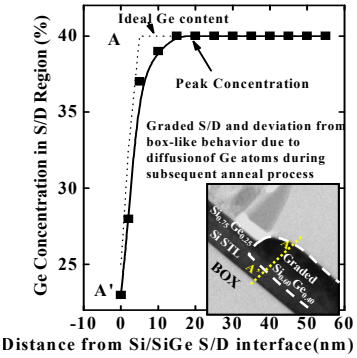

Fig. 4. Auger Electron Spectroscopy depth profile of Ge content in the graded embedded $Si_{0.6}Ge_{0.4}$ S/D. Grading of S/D aimed to minimize misfit dislocation nucleation .

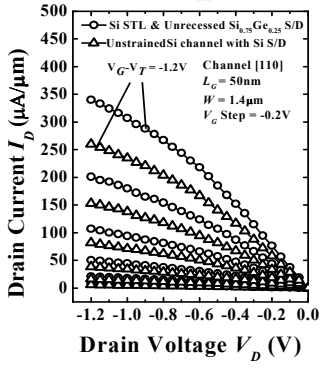

Fig. 5. Plot of I_D-V_D for ***Devices (a)*** and ***(c)*** $I_{D,sat}$ enhancement of 30% is observed. Due to the higher hole mobility supported by the SiGe channel, drive current is enhanced.

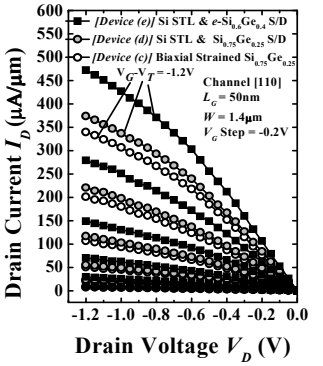

Fig. 6. Plot of I_D-V_D for ***Devices (c), (d)*** and ***(e).*** $I_{D,sat}$ enhancement of 13% is observed when $Si_{0.75}Ge_{025}$ interacts with Si STL. 54% enhancement is achieved with recessed graded $Si_{0.6}Ge_{0.4}$ S/D

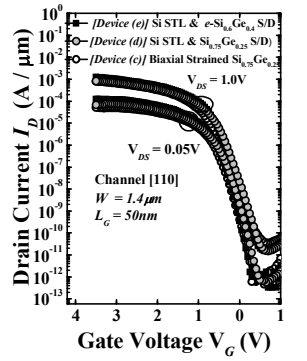

Fig. 7. Plot of I_D-V_G for ***Devices (c), (d),*** and ***(e).*** Similar *DIBL* and subthreshold characteristics were obtained for the devices, justifying comparison.

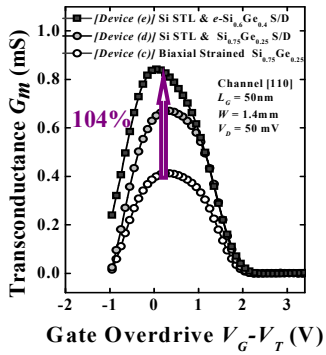

Fig. 8. Plot of G_m-(V_G–V_T) for ***Devices (c), (d),*** and ***(e).*** A G_m enhancement of 104% was observed in graded ***e***-$Si_{0.6}Ge_{0.4}$ S/D (***Device (e)***) over unrecessed $Si_{0.75}Ge_{025}$ S/D device

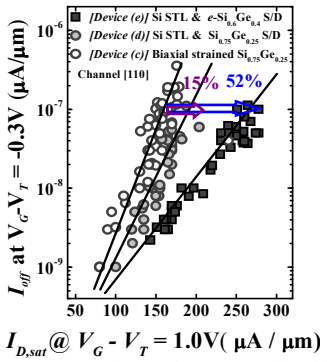

Fig. 9. At I_{off} of 100nA/um, a saturation drive current enhancement of 52% is achieved for ***Device(e)*** and 15% for ***Device (d).*** over unrecessed $Si_{0.75}Ge_{025}$ S/D device.

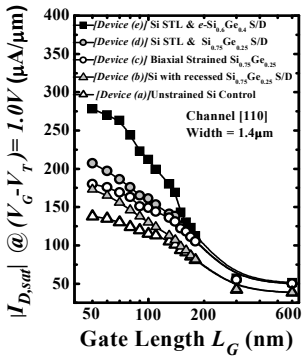

Fig. 10. Plot of drive current as a function of L_G for various schemes of strained devices with different stressors incorporated.

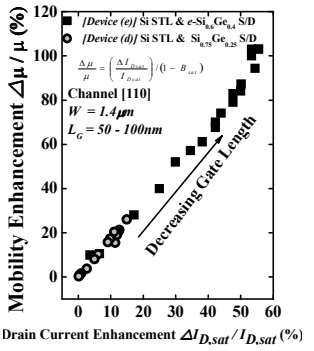

Fig. 11. Significant $I_{D,sat}$ enhancement observed in ***e***-$Si_{0.6}Ge_{0.4}$ S/D device, is attributed to the large gain in hole mobility and strain induced in channel.

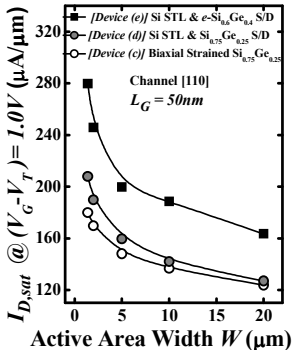

Fig. 12. . Narrower width results in relaxation of in plane compressive strain perpendicular to channel direction and affects *p*-FET drive current.

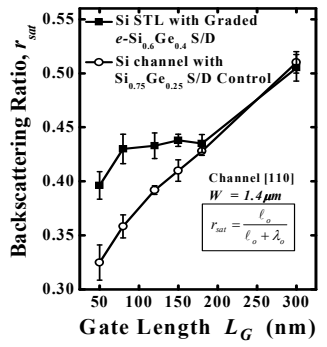

Fig. 13. Impact of strain on extracted r_{sat} for various L_G. *Higher* r_{sat} is observed for strained devices Despite more channel backscattering in strained devices, drive current was enhanced

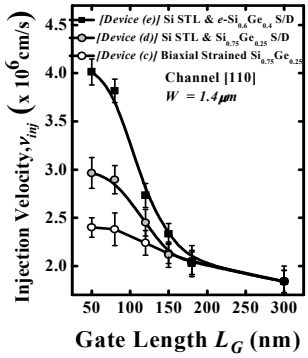

Fig. 14. Higher r_{sat} results in degradation of B_{sat} Much higher v_{inj} compensates B_{sat} redction in strained devices, resulting in a net gain in drive current.

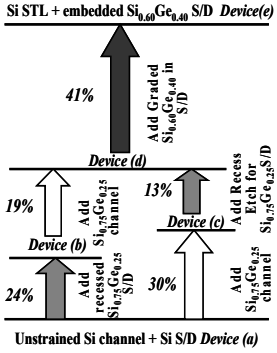

Fig. 15. Summary of device performance enhancement, illustrating the effectiveness of Si STL in channel strain modulation.