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New Observations on the Narrow Width Effect of the Hot Carrier and NBTI Reliabilities in pMOSFETs with Various Types of Strains

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Abstract- In this paper, we present new results on the width dependent hot carrier reliability and/or NBTI degradation for shallow-trench isolated (STI) on the uniaxial and biaxial strained pMOSFET devices. In p-MOSFET's, the interface traps generation at the STI-edge is enhanced for narrow width device. It was found that uniaxial (SiGe S/D) strained structure has comparable HC reliability with biaxial (SiGe-channel) device for long channel devices, while the drain current degradation is more enhanced for a reducing gate width in **uniaxial narrow width** strained device. This is related to the **tensile stress** in the channel width direction compared to the compressive stress of STI in **biaxial strained** SiGe channel devices. This **tensile stress** results in a much worse reliability. For NBTI reliability, it was found that the STI strains are strongly related to the channel width. This is a very crucial issue for the present and future CMOS ULSI using STI technologies in the narrow width strained devices.

Keywords: shallow trench isolation (STI), HC reliability, Inverse Narrow Width Effect (INWE), negative bias temperature instability (NBTI), Strained-Si device

Introduction- In more recent years, strained-Si devices in the channel [1-2], SiGe source/drain [3-4], and hybrid substrate technology [5-7] have been attractive for high speed and low power logic CMOS technologies. With the scaling down of CMOS technology, MOSFET characteristics become more sensitive to the device narrow-width shallow trench isolation (STI), which exhibits severe degradation after hot-carrier (HC) stress with a reducing gate width. STI induced strain has been shown to have a significant impact on bulk device performance [8][9]. These effects could affect the uniaxial and biaxial narrow width strained-Si performance especially in the narrow width devices. However, there are several other issues that become significant with device scaling. According to experimental observations, devices with the STI/gate edge in narrow width strain device exhibit different degradation mechanisms at various temperatures. Generally, the negative bias temperature instability (NBTI) in pMOSFETs is attributed to the generation of interface traps and oxide trap charges [10].

In this paper, the degradation mechanisms resulting from different strained engineering and substrate engineering with a reducing gate width have been extensively studied. Their hot carrier and NBTI (Negative Bias Temperature Instability) reliabilities have been verified and the associated mechanisms have been extensively studied.

I. Device Preparation

For the experimental work in this paper, the devices were fabricated using the 65-nm foundry advanced CMOS technology. For the pMOSFETs, SiGe-channel, SiGe S/D with <110> channel was made on (100) substrate. Device has either 16Å (physical thickness) or 14Å SION gate oxide.

II. Results and Discussion

A. *Width Dependence of the Threshold in pMOSFET*

The tested devices are the SiGe-channel and SiGe S/D pMOSFETs in Fig. 1 and the comparison with control-Si devices. Fig. 2 shows V_t as a function of width for a gate length of 0.12 um, comparing to W = 10um. The Vt in the control-Si and SiGe S/D device show that Vt first increases slightly to a maximum and then decreases rapidly as width decreases. From [11], we know that the compressive stress tends to increase Vt. The Vt reduces slightly under width= 0.2 um is due to the well-known inverse narrow width effect (INWE). For the SiGe-channel device, Vt increases significantly with decreasing width. The difference in the Vt trend for it has been found to be different in that a much strong anomalous narrow width effect near the STI/gate edges [12] for SiGe biaxial strains. Again, Fig. 3 shows drain current decreases as a function of reducing channel width for the control-Si and SiGe S/D devices, while we see a huge increase in biaxial strained SiGe-channel devices. The current enhancement in biaxial strained device is greatly improved.

B. *Hot-Carrier Studies on Narrow Width Strained pMOSFET*

Various widths stressed configuration and their associated stressing effects caused by STI-enhanced hot carrier area have been illustrated in Fig. 4. The longitudinal compressive stress and transverse compressive stress are applied on SiGe-channel device, 4(c), while the longitudinal compressive stress and transverse tensile stress are applied on SiGe S/D device, 4(d), in pMOSFETs [13]. In Fig. 4(c) and Fig. 4(d), the STI will increase transverse compressive stress in narrow width strained devices. Figs. 5 and 6 show the I_D degradation for (100) and (110) substrates with either control or strained SiGe-channel. Both indicate that (110) substrate devices have lager degradation, since silicon and oxygen atom bonding energy is weaker for (110) orientation substrate devices [14]. Figs. 7 and 8 show that SiGe S/D narrow width strained structure has a much worse reliability due to its transverse tensile stress (Fig. 4(d)). On the other hand, as we see from Fig. 9, it reveals that SiGe S/D has lower impact ionization rate (I_B/I_D). Therefore, the impact ionization rate (I_B/I_D) is not the dominant degradation factor in a narrow width strained device.

C. *Observation of Narrow Width Strained pMOSFET Dependent NBTI Effect*

Fig. 10 shows the threshold voltage shift under NBTI stress. The SiGe S/D uniaxial narrow width strain shows much better NBTI characteristics compared to SiGe-channel biaxial narrow width strain device. It is attributed to the generated SiGe defects in the channel in SiGe-channel devices. It can be further justified from Fig. 11 in that SiGe-channel device has smaller activation energy. Also, we have seen the results under NBTI like-HC stress, it was found that the strain device exhibits much worse width dependent degradation at high temperatures as given in Fig. 12. This implies that NBTI performance in the narrow width strain devices is a major problem for either types of strained techniques.

In summary, new results on the width dependent hot carrier reliability and/or NBTI degradation for shallow-trench isolated (STI) structure with various strains have been extensively studied. In terms of the HC reliability, it was found that the drain current degradation is more enhanced **for a reducing gate width** in **uniaxial** strained devices, comparing to the biaxial ones. For the NBTI reliability, it was found that the strain devices exhibit much worse width dependent degradation at high temperatures. As a consequence, it sets a limit to a high performance design of logic CMOS devices with strained technologies.

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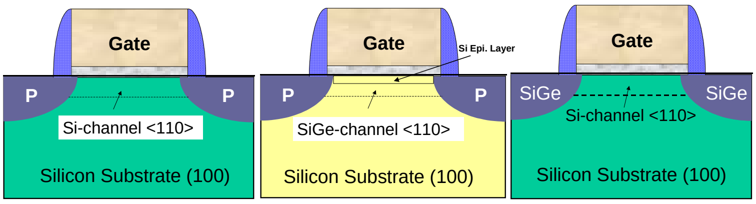

(a) Control (b) SiGe-channel (c) SiGe S/D

Fig.1 The cross-sectional views of (a) bulk-Si device, (b) SiGe-channel, and (c) SiGe Source/drain compressively strained pMOSFETs.

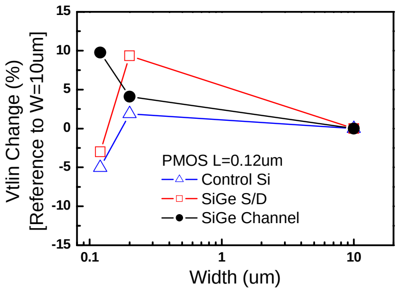

Fig. 2 Comparison of the $V_{t,lin}$ (%) variation with channel width for three devices given in Fig. 1.

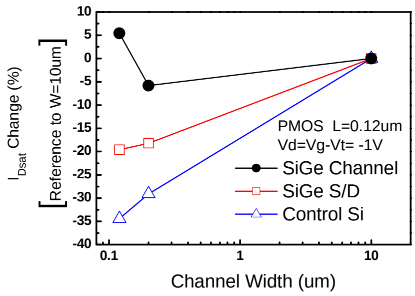

Fig. 3 Comparison of the I_{Dsat} (%) variation with channel width for three devices given in Fig. 1.

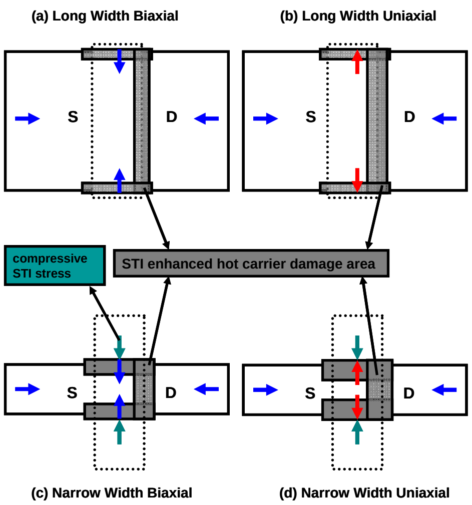

Fig. 4 Various of width stress configuration and their associated stressing effects induced at different STI enhanced hot carrier areas.

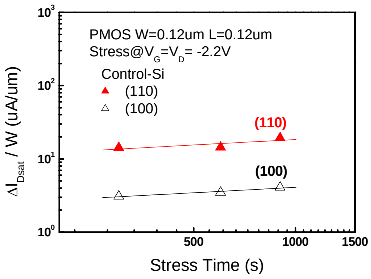

Fig. 5 The drain current degradation for (100) and (110) orientations devices in long width under HC stress at V_G= V_D= -2.2V.

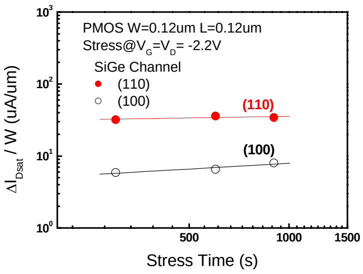

Fig. 6 The drain current degradation for (100) and (110) orientations devices in narrow width under HC stress at V_G= V_D= -2.2V.

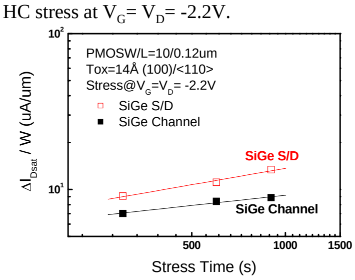

Fig. 7 The drain current degradation for SiGe-channel and SiGe Source/drain devices in long width under HC stress at V_G= V_D= -2.2V.

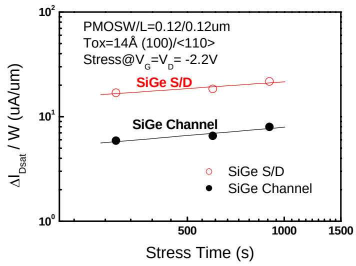

Fig. 8 The drain current degradation for SiGe-channel and SiGe Source/drain devices in narrow width under HC stress at V_G= V_D= -2.2V.

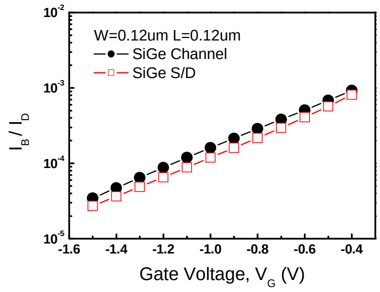

Fig. 9 Comparison of the impact ionization rate(I_B/I_D) for SiGe-channel and SiGe Source/drain.

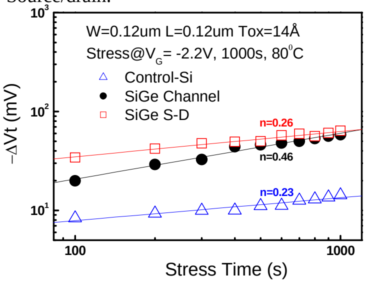

Fig. 10 Comparison of the threshold voltage shift under NBTI stress for three devices given in Fig. 1.

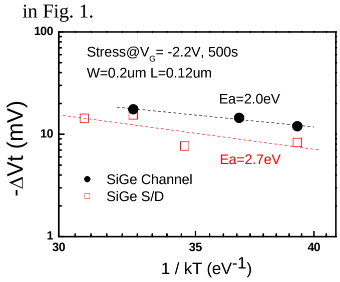

Fig. 11 Comparison of the activation energy for SiGe-channel and SiGe Source/drain.

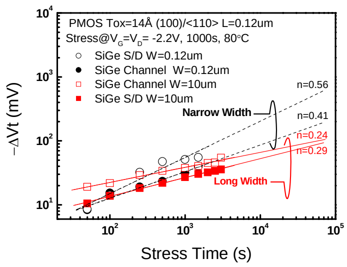

Fig. 12 The drain current degradation for SiGe-channel and SiGe Source/drain devices with various widths under NBTI like-HC-stress.