Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 898-899

B-10-2

Analysis of Random Telegraph Signal Noise in Dual and Single Oxide Device And Its Application to CMOS Image Sensor Readout Circuit

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1. Introduction

As the device dimensions continue to shrink with each new generation of MOS technology, the effect of an individual defect on device performance becomes more pronounced. Due to trapping and detrapping of electrons from a single oxide trap, the drain current changes discretely, known as random telegraph signal (RTS) noise [1]. RTS noise gives a negative effect on a lot of analog circuits. Especially, the performance of CMOS image sensor (CIS) is limited by such a low frequency noise. It is well-documented that the source follower of the CIS readout circuit is a dominant low frequency noise source [2]. Through experiments, we found that there is a different RTS noise characteristic between dual and single oxide devices. In this paper, for the first time, distribution of RTS noise amplitude was statistically extracted from dual and single oxide devices and we applied the results to CIS readout circuit in order to make a conclusion of which one is more suitable for reduced output noise.

2. Results and Discussion

Experiments were performed for two different wafers. One was fabricated with dual oxide process that consists of 0.7 nm bottom gate oxide and 4.1 nm top gate oxide. The other one was fabricated with single oxide process which has 4.8 nm gate oxide thickness. From each wafer, we selected 50 source follower transistors, $0.40\mu m$ in width and $0.32\mu m$ in length, and measured drain current noise, whose results are shown in Fig. 2 (a). Given the bias condition of Fig. 1, most devices show two level drain current fluctuations. RTS noise amplitude was statistically extracted by using histogram of time domain data. Because of two level current, dual Gaussian distribution was observed, as in Fig 2 (b). By using the above method, we extracted RTS noise amplitude of 50 devices from dual and single oxide wafer. Fig. 3 represents both cases of RTS noise distribution. In the dual oxide devices case, RTS noise amplitude for 78% of devices were less than 20 nA. On the contrary, in case of single oxide devices, only 58% was less than 20 nA, which indicates that single oxide devices have more severe RTN than dual oxide devices.

In Fig. 1, M3 plays a role as a current source which offers constant current through M1 and M2. Therefore, RTS noise phenomenon of M2 would be occurred as a voltage fluctuation of source node of M2 instead of current fluctuation. RTS noise current fluctuation in Fig. 3 was converted to voltage fluctuation value by using transconductance of M2 at the given bias condition. Experimentally, $g_m = 37.73\mu A/V$ was measured.

Through the pass transistor M4, voltage at the source node of M3 transfers to the V_{out} node without any voltage drop because high voltage V_{DD} is biased at the gate of M4. As a result, it was possible to obtain a cumulative probability curve at V_{out} node, which is shown in Fig. 4. Instantly, it can be recognized that RTN of single oxide devices is higher than that of dual oxide devices. Average values of output noise from dual oxide M2 and single oxide M2 were $500\mu V$ and $599\mu V$, respectively. Especially, in case of single oxide device, a very large nose voltage of 1.95 mV was observed in a device.

In addition to time domain data, power spectrum density (PSD) also describes noise behavior of dual and single oxide devices, which are shown in Fig. 5. Large variation in PSD was observed in the devices due to small area. Using Fig. 5, we calculated average value of PSD as shown in Fig. 6. Under the 1000 Hz, PSD of single oxide device is higher.

By virtue of both time domain and frequency domain data, we can make a conclusion that single oxide devices cause more severe voltage variation at V_{out} node than dual oxide devices do. This is mainly related to trap depth. We extracted the trap depth of 10 devices from dual and single oxide wafer, through the equation (1) and the procedure in Fig. 7.

$$x_T = -T_{ox}\frac{kT}{q}\frac{d\ln(\tau_c/\tau_e)}{dV_{gs}} \qquad (1)$$

Where, T_{ox} is oxide thickness and kT/q=0.0259 V, τ_c is capture time and τ_e is emission time. Fig. 8 (b) shows trap depth distribution of both dual and single oxide devices. Apparently, traps in single oxide are closer to the Si-SiO_2 interface than traps in the dual oxide case. In dual oxide case, second oxidation generates additional oxide layer which is 0.6 nm~0.8 nm thick. Therefore, the trap depth distribution became larger from Si-SiO_2 interface. The average value of trap depth in dual oxide is 2.84 nm and that of single oxide is 2.12 nm. The difference of trap depth between single and dual oxide device is coincidence with second oxidation thickness. Generally, when trap are closer to the Si-SiO_2 interface, RTS noise amplitude increases due to increase in scattering effect. Fig.8(a) shows experimental data of the relationship between trap depth and RTS noise amplitude.

3. Conclusions

Distributions of RTS noise amplitude were extracted from dual and single oxide devices. Experimentally, single oxide

devices have larger RTS noise which causes larger voltage variation in the output node of a CIS readout circuit. The results give an sight for designing device with better gate oxide characteristic.

Acknowledgements

This work was supported by Samsung Electronics.

References

[1] M.J Uren *et al., Adv. Phys., Vol.38, pp.367, 1989.*

[2] Xinyang Wang et al, *"Random Telegraph Signal in CMOS Image Sensor Pixels", in IEDM Tech, Dig., 2006, no.4.*

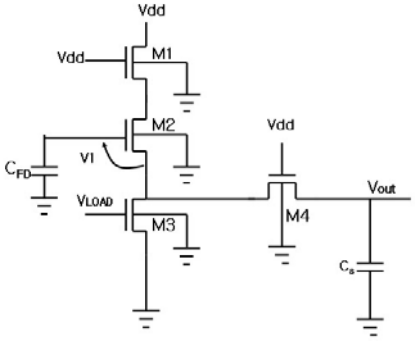

Fig. 1. Bias conditions are represented in CIS readout Circuit. Current Source M3 maintains $3\mu A$ and M2 is a dominant low frequency noise source.

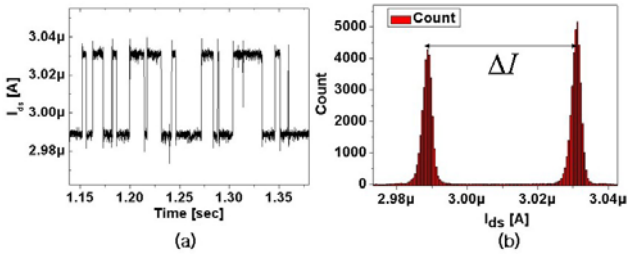

Fig. 2. (a) RTS noise time region behavior (b) amplitude.

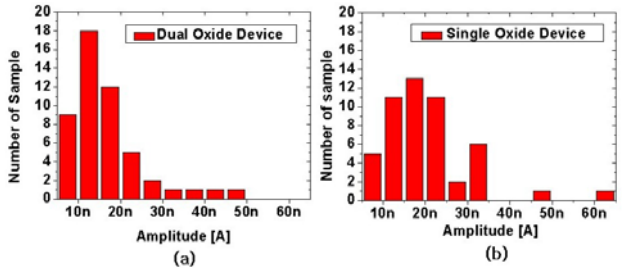

Fig. 3. (a) RTS noise amplitude distribution in dual oxide devices (b) in single oxide devices.

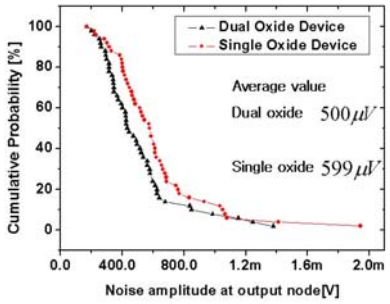

Fig. 4. Cumulative probability at output node which is caused by RTS noise of M2.

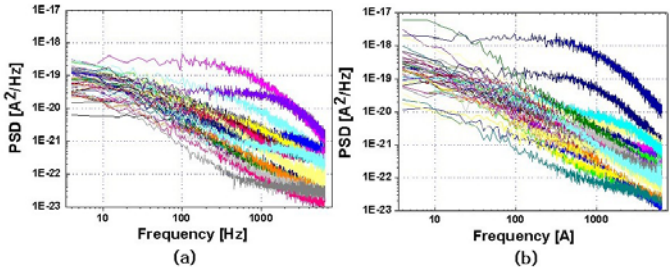

Fig. 5. (a) PSD from dual oxide devices (b) PSD from single oxide devices.

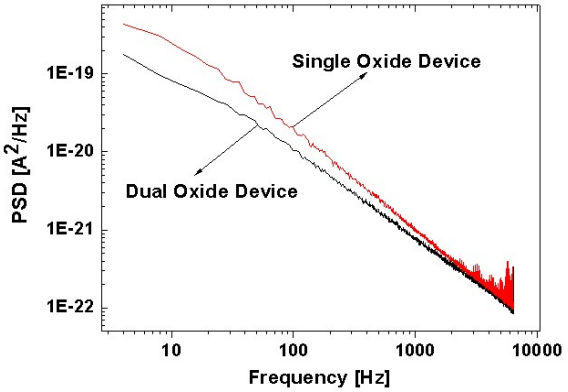

Fig. 6. Comparison of average PSD in dual oxide devices with average PSD in single oxide devices.

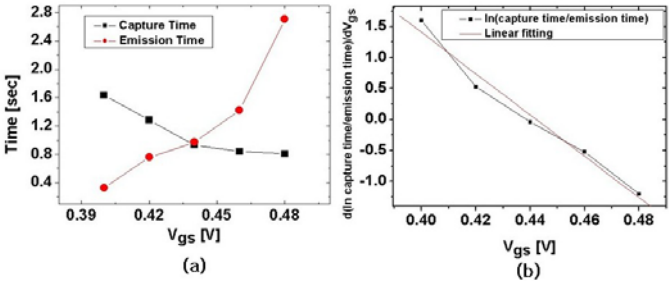

Fig. 7. Process of extracting trap depth (a) Time constant variation with respect to V_{gs} (b) Extraction of $d\ln(\tau_c/\tau_e)/dV_{gs}$ through linear fitting.

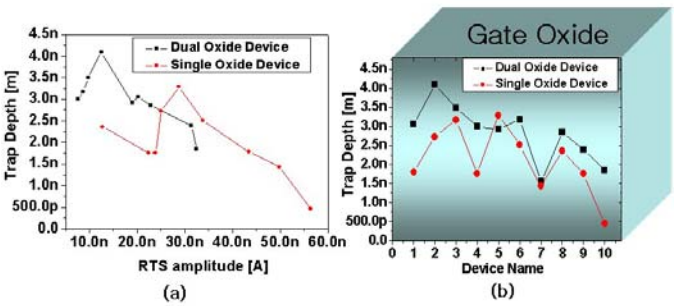

Fig. 8. (a) Relationship between trap depth and RTS noise amplitude. As trap depth increases noise amplitude decreases. (b) Distribution of trap depth in dual and single oxide device.