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Analog Performance of Asymmetric Schottky Tunneling Source nFET for RF and Mixed-Mode Application

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1. Introduction

The demand for increasing computing and communication applications has driven efforts to integrate analog functions with their digital counterparts, resulting in high performance system on chip (SOC). While continuous scaling of conventional CMOS makes it an excellent choice for RF wireless communications, due to increased short channel effects (SCE), the output resistance (R_{OUT}) of sub-100 nm MOSFETs degrades significantly. This severely reduces the intrinsic gain of the device. It is becoming increasingly difficult to achieve both high gain and high f_t simultaneously in conventional devices as seen in Fig. 1 [1]. New approaches to avoid this limitation have to be explored to achieve a high frequency transistor with good gain performance.

In this paper, a novel asymmetric Schottky Barrier tunneling FET introduced in [2, 3] with gate modulated Schottky Barrier source tunneling is investigated to improve MOSFET analog performance down to sub-100 nm regime.

2. Device Structure

Schottky Barrier transistors are one of the primary candidates that can be used for mixed mode applications due to significant improvement in their scaling properties and parasitic reduction [4, 5]. Fig. 2 shows the device structure of the asymmetric Schottky Tunneling Source nMOSFET (STSFET). The device uses fully silicided S/D junctions with a highly doped n+ pocket at the drain side. The operating principle of the STS FET utilizes the concept of gate-controlled Schottky Barrier tunneling between the source silicide and the channel Si as shown in Fig. 3 [6]. Transistors with Schottky Barrier source have the advantage of reduced SCE compared to conventional MOSFETs. Extensive simulations were performed using the Synopsys-TCAD tool, DESSIS device simulator which takes into account Schottky barrier tunneling, to understand the detailed characteristics of this device.

3. Discussions

I. Optimization of device parameters

For Schottky source junction with large source junction Barrier Height φ_b, the sub-threshold region is controlled by Schottky Tunneling mechanism [2]. The I_{ON} is therefore reduced by the tunneling junction resistance. In the case of low φ_b (<0.25eV) the sub-threshold current is controlled by diffusion mechanism, just like a conventional MOSFET, and the advantages of reduced SCE disappear [2]. Thus, an intermediate φ_b = 0.45eV was chosen to ensure the subthreshold current is limited by tunneling, but without excessive I_{ON} reduction. The oxide thickness was decreased to reduce the subthreshold swing. The sub-threshold swing (which has a weak temperature and scaling dependence) shows a linear dependence on oxide thickness as shown in Fig. 4. A small EOT of 5Å was chosen to maintain a reasonable swing (~80mV/dec). The Si-film thickness is fixed at 25nm. The n^+ pocket ($N_D = 1x10^{20}/cm^3$) at the drain junction eliminates the potential drop at the drain side Schottky Barrier which degrades the current at low V_D. Fig. 5 shows the improvement in the linear region for the I_D-V_D characteristics of the device.

Fig. 6 shows the threshold voltage (V_{th}) roll-off and the Drain Induced Barrier Lowering (DIBL) of the STSFET as compared to SOI-FETs. As the Schottky Barrier Height (φ_b) increases, the SCE improve drastically. For φ_b = 0.45eV, we see that DIBL and V_{th} roll-off is much improved as compared to SOI-FETs. The reduced SCE are due to the fact that the drain field has very little effect on the source side Schottky Barrier as seen in Fig. 7. This explains the high immunity to DIBL for the STSFET, since its subthreshold current is limited by the Schottky Barrier tunneling.

II. Analog Performance

The transconductance (g_m) of the STSFET at different L_G's is shown in Fig. 8. Fig. 8 (inset) indicates that the STS-nFET has a slightly lower g_m at a given bias current (with V_D = 0.8V) than conventional SOI-FET. This decrease is due to the tunneling resistance of the Schottky Barrier at the source end. This also explains the slight reduction of I_{ON} in the STSFET as compared to a conventional FET.

However, as seen in Fig. 9, there is a drastic improvement in R_{OUT} as compared to conventional SOI-FET for L_G = 90nm and 50nm (V_D is set at 0.8V). Since the drain voltage has only a small effect on the electron tunneling across the Schottky Barrier at the source side as mentioned above, DIBL is greatly reduced. As a result, R_{OUT} improves. As expected, R_{OUT} reduces with increasing bias current, just as in a conventional FET due to channel length modulation effects.

Fig. 10 shows the intrinsic gain ($g_m x R_{OUT}$) performance of the STSFET as compared to a conventional SOI-FET. There is a net improvement in gain of about one order of magnitude due to the substantial increase in output resistance as explained above. When the STSFET is scaled to 50nm, a gain of close to 100 is obtained for bias currents as high as 500μA/μm.

The Frequency-Gain performance of the STSFET is shown in Fig. 11. It can be seen that under the same bias current (100μA/μm) condition, the STSFET has intrinsic gain almost an order higher at the same f_t for different generation nodes. Even with a higher bias current (400μA/μm), the frequency gain performance of the STSFET is exceptional as shown in Fig. 12.

4. Conclusions

The novel asymmetric Schottky Tunneling Source nMOSFET utilizing the concept of gate controlled Schottky barrier tunneling has been examined in detail with respect to its analog performance. It has been shown that the STSFET shows excellent short channel immunity and reduced DIBL. Additionally, the output resistance of the STSFET is increased by almost an order over conventional FETs. Therefore, the STS-FET has a much higher gain-frequency performance even for sub-100nm generation nodes. This makes the Schottky Tunneling Source FET a promising candidate for RF and mixed mode applications

5. Acknowledgements

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References

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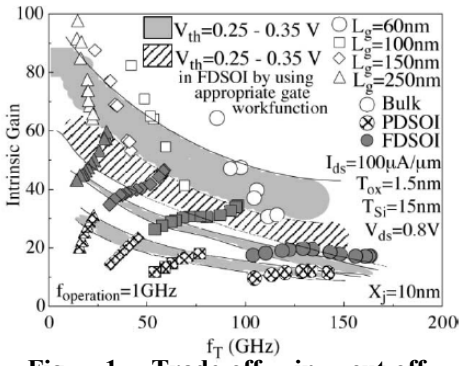

Fig. 1 Trade-off in cut-off frequency and intrinsic gain in conventional MOSFET devices [1]

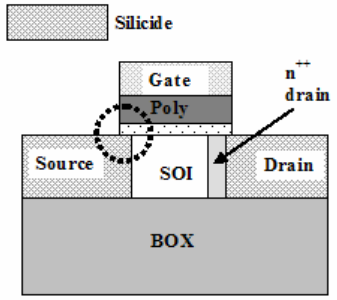

Fig. 2 Device structure of the asymmetric STS n-MOSFET

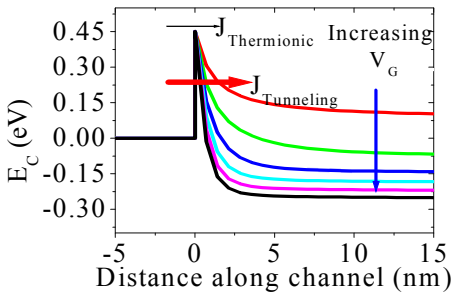

Fig. 3 Conduction band edge profile along the channel length for STS n-FET

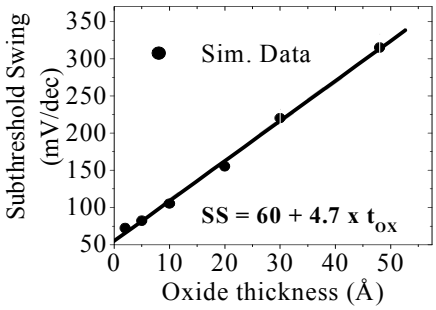

Fig. 4 Sub-threshold Swing for different t_{OX}. A linear fit is observed with the equation inset

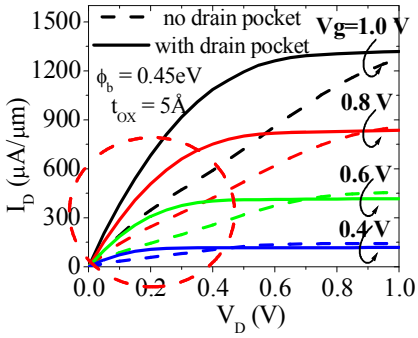

Fig. 5 Improvement in the linear region I_D-V_D characteristics due to the presence of n^+ drain side pocket

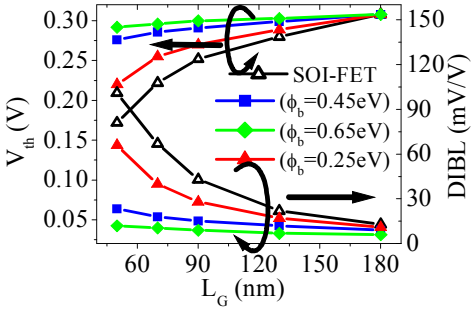

Fig. 6 V_{th} roll-off and DIBL for the STS-nFET at different φ_b as compared to conv. SOI-nFET

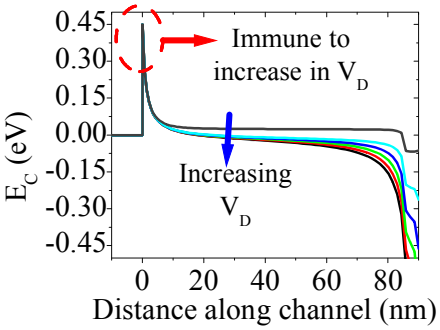

Fig. 7 Conduction band edge along the channel for different V_D

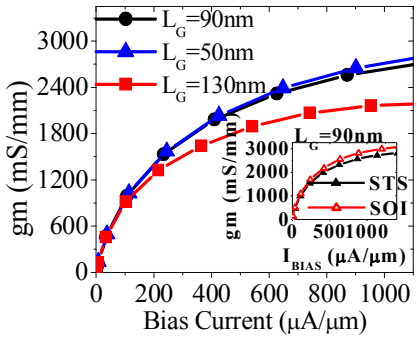

Fig. 8 Transconductance as a function of bias current for different L_G's. Inset: Comparison of gm between STS and SOI FET for L_G=90nm

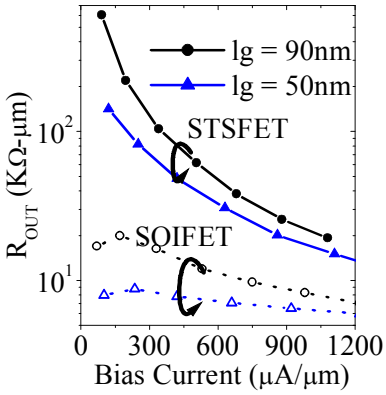

Fig. 9 Comparison of R_{OUT} vs bias current for two different L_G's for the STS and the SOI FETs

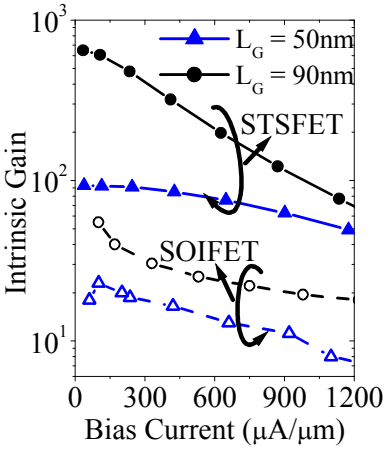

Fig. 10 Intrinsic Gain at different bias currents for two different L_G's for the STS and SOI FET

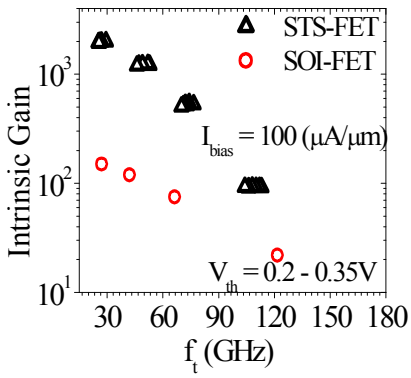

Fig. 11 Comparison of f_t – Intrinsic Gain performance for STS and SOI FET at I_{bias} = 100μA/μm

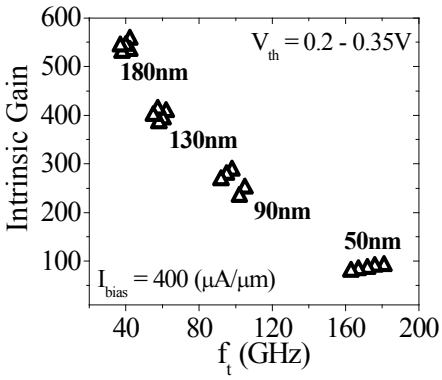

Fig. 12 f_t – Intrinsic Gain performance of the STSFET at a higher I_{bias} = 400μA/μm