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Low Standby Power CMOS Process Integration Scheme for 45-32 nm node

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1. Introduction

Low standby power (LSTP) chips have been widely implemented for battery-operating low-activity low-cost consumer type applications, with an emphasis on the lowest possible leakage current. Today, high-performance element such as digital TV and web browsing are being integrated into the cellular phones (Fig.1), and LSTP chips are required to have a multiple performance of low-leakage, high-speed, and low-dynamic power. In order to reduce leakage current, however, LSTP transistor commonly require a higher threshold voltage, a thicker gate dielectric film, a lower extension/halo doping, which in turn limit drive current.

Latest technologies, such as mobility enhancement, high-k gate dielectric film and metal gate electrode, will be introduced to LSTP devices, since these are able to improve drive current without increasing leakage current. In this paper, I will discuss the appropriate technologies for 45-32 nm node LSTP CMOS from process cost point of view.

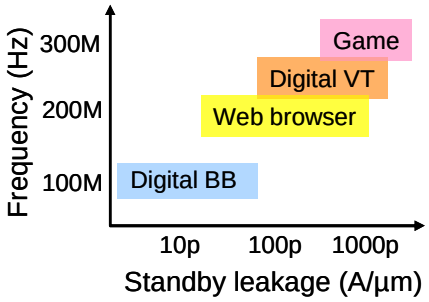

Fig. 1 LSTP chips are required to integrate multi-functional elements.

2. Mobility enhancement methodology for LSTP CMOS

HP CMOS utilizes <110> direction channel, which has good compatibility with process-induced strain technologies such as embedded SiGe and dual stress liner (DSL) [1-2]. Restrictive DFM rules are required to obtain sufficient mobility enhancement effect, however, this limit the gate density. On the other hand, LSTP CMOS commonly utilizes <100> direction channel in which mobility is less sensitive to layout patterns [3], so that higher gate density with less restrictive layout rules can be realized. However, the mobility enhancement with process-induced strain is less effective in this case.

We propose another mobility enhancement approach designed for LSTP CMOS. Carrier mobility in LSTP CMOS is strongly affected by impurity scattering because of higher channel doping concentration required for high threshold voltage, i.e., low subthreshold leakage current. To mitigate the above issue, we have introduced gate work function (WF) modulation technique, exploiting Fermi-level pinning phenomenon with high-k material "hafnium" deposited on SiON film [4-5]. This technique requires only a few process steps added to conventional fabrication sequence. Figure 2 shows saturation transconductance curves with two different threshold voltage control method; (a) channel doing concentration, (b) WF modulation with hafnium. By using WF modulation, the maximum value of transconductance does not degrade even at higher threshold voltage. In order to sustain channel doping controllability for multi-threshold voltage ranged 0.5V to 0.3V, preferable Vth increase amount by WF modulation is 0.2V as shown in Fig.3.

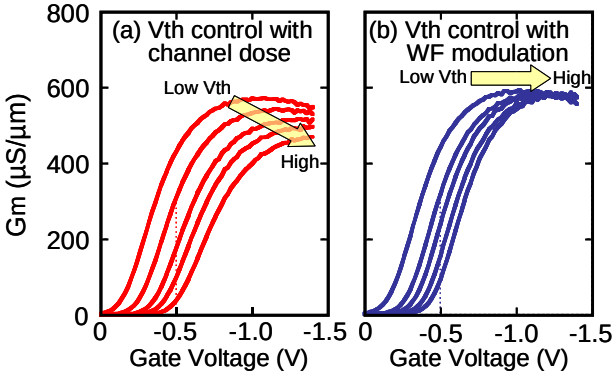

Fig.2 Saturation transconductance curves with two different threshold voltage control method; (a) channel doing concentration, (b) WF modulation with hafnium.

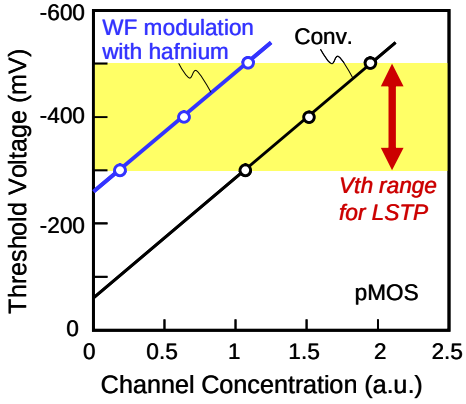

Fig.3 By using WF modulation, channel doping concentration effectively reduced while maintaining multi-Vth controllability.

3. Process and design methodologies for low-leakage

WF modulation technology also reduces leakage current such as GIDL and junction leakage current. Figure 3 shows standby leakage current as a function of threshold voltage. GIDL becomes dominant in standby leakage current as threshold voltage becomes high. Work function modulation accompanied with reduced channel doping effectively reduces GIDL, resulting in reduced standby

leakage current.

To reduce standby leakage current further, supply voltage may be brought down to around 0.7 V, the voltage at which SRAM data are still retainable at the standby mode. We can reduce subthreshold leakage current to 5pA or less with this method, even from initial subthreshold leakage of 50 pA at 1.1 V.

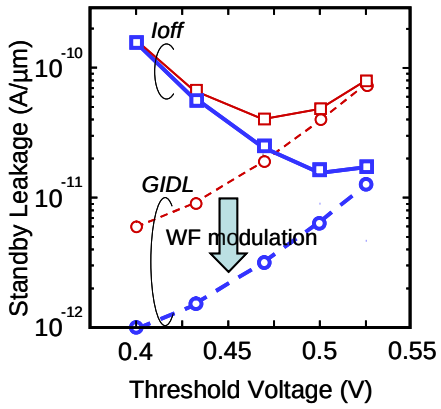

Fig.4 Off-state standby leakage current and GIDL as a function of threshold voltage

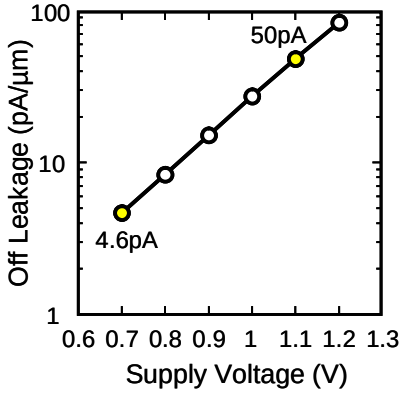

Fig.5 Off-state leakage current effectively reduces with lowering power supply voltage.

4. Dual core technology for low active power

In order to reduce operating power of high activity portion on a chip, we have introduced dual core process with which both LSTP and LOP transistors can be fabricated. The only difference between LOP and LSTP is the gate dielectric thickness; LSTP transistors has 1.8 nm-thick gate oxide for 1.1-1.2 V operation, while LOP transistors with 1.3 nm-thick gate oxide for 0.9-1.0V operation. LOP transistor has 14-16 % of higher on-current than LSTP at the supply voltage of 0.9 V. Target specification of each transistor is summarized in Table 1.

Table 1 45nm node device performance summary

	LSTP			LOP
Vdd (V)	1.1			0.9
EOT (nm)	1.8			1.3
Lg (nm)	40			40
Jg (A/cm²)	0.05			5
Ion (μA/μm)	745/374	610/308	476/247	620/310
Ioff (A/μm)	5n	500p	50p	5n

5. Metal gate suitable for LSTP CMOS

Metal gate will be indispensable technology for 2nd generation of 45 nm or 32 nm LSTP CMOS. Figure 6 shows preferable metal work functions for LSTP CMOS. Both thinner Tinv and WF modulation contribute to random variation suppression as well as on-current improvement. Figure 7 shows Monte Carlo simulation result of threshold voltage variation with (a) polysilison/SiON (tinv=2.6nm), (b) polysilicon/Hf/SiON (tinv=2.6nm), and (c) metal/high-k/SiON (tinv=1.8nm). Estimated σVth is (a) 23.8mv, (b)18.1mV, and (c)14.5mV, respectively.

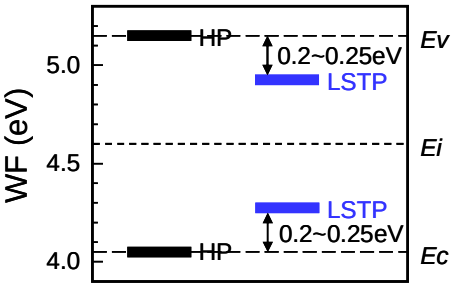

Fig. 6 Preferable metal work-function for LSTP applications

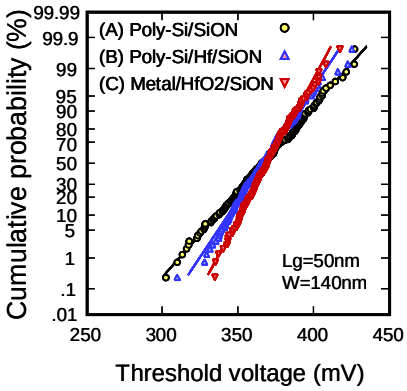

Fig.7 Monte Carlo simulation result of threshold voltage variation with three different gate electrode structures

5. Conclusions

Process integration scheme for 45-32 nm node LSTP CMOS have been discussed. WF modulation is a very cost-effective approach for drive-current improvement as well as leakage reduction in current generation. Metal gate will be indispensable for next generation LSTP CMOS for further performance improvement and variability suppression.

Acknowledgements

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