B-3-2

High Performance and Low Leakage CMOS for 45nm Low Power Technology and Beyond

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Introduction

The push for greater performance, while maintaining low power has been driven by the rapid growth of portable handheld electronics where enhanced multimedia delivery & extended battery life are highly desired. To this end, traditional scaling of the gate oxide for performance is limited without the implementation of high-k gate dielectrics as gate leakage becomes a significant component of overall leakage. An effective approach which meets both the performance and low power goals is stress-induced carrier mobility enhancement, including dual stress liner (DSL) [1], stress memorization technique (SMT) [2], stress proximity technique (SPT) [3, 4] and eSiGe [5, 6].

In this paper, we combine the various elements of strain enhancement to deliver a best-of-class low power process which meets both the stringent requirements of performance as well as leakage. We are able to obtain (1) best reported pFET performance at Vdd=1.1V; (2) improved pFET V_T roll-off ; (3) significant reduction of ring oscillator delay even at the minimum contacted poly gate pitch; (4) largely reduced GIDL leakage current with optimized implant condition; (5) noticeable nFET enhancement; and (6) non-degraded parasitic characteristics.

The success of achieving high performance and low leakage with strain engineering without high-k metal gate for 45nm low power technology opens a viable option for future technologies.

Experimental

The devices used in this study are fabricated based on a 45nm low power CMOS bulk technology on (001) substrates with <110> channel. Main device features consists of a 1.8nm (EOT) plasma nitrided gate oxide, 100nm poly-Si gate of gate length down to 40nm, optimized eSiGe and DSL. Control samples have similar elements and features including DSL except eSiGe stressor. Figure 1 illustrates the process flow used in this study. A cross-section of a typical pFET after final processing is shown in Fig. 2; The average Ge profile ~22% (at. %) for the eSiGe (not shown here) was determined by Auger Electron Spectroscopy (AES).

Results and Discussions

The benefit of eSiGe on pFET performance is well documented [7, 8]. However, this enhancement typically comes with trade-offs in elevated parasitic leakages. Our analysis is focused on maximizing performance gain while maintaining the low levels of leakage expected of a low power process.

Advanced 45nm low power CMOS integration with implementation of eSiGe S/D and dual stress liner (DSL) has been successfully demonstrated. The Ion-Ioff characteristic of the pFETs with eSiGe shows a performance gain of 40% over control. A drive-on current of 530 μA/μm is obtained for a device width of 0.3 μm at Ioff = 1 nA/μm with a poly pitch of 182nm and a Vdd of 1.1V. Two reference values of devices, one with eSiGe at a 65nm poly pitch and a Vdd of 1.2V [9] and another without eSiGe but with 45° rotated substrate at a 45nm poly pitch [10], fall behind our results in Fig. 3.

In order to identify the major contribution to the observed drive-on-current enhancement, the pFET resistance at fixed gate overdrive (Rodlin) is plotted in Fig. 4. The reduction in the slope of the Rodlin vs. Lpoly indicates an enhancement in the short channel hole mobility of more than 30% with eSiGe. Improved pFET SCE is also observed with eSiGe as seen in Fig. 5. PFET linear current at fixed gate overdrive (Iodlin) as a function of device width, as shown in Fig. 6, indicate a large enhancement of Iodlin for the pFETs with eSiGe even at narrow device width.

NFET performance is enhanced by ~8% on devices with both channel width of 0.3 μm (s. Fig. 7) and 2 μm (not shown). This may attribute to the additional thermal steps and hydrogen species from eSiGe process. The area junction capacitance (s. Fig. 8) with eSiGe process is similar to control, while the sidewall capacitance (s. Fig. 8) is reduced by 20%. B diffusion in eSiGe is slower than in Si, therefore more graded profile of B in Si and optimized implantation help in the reduction of Cjswg, The effect of eSiGe on the ring oscillator performance at minimum contacted poly gate pitch is evaluated; approximately 25% reduction in ring oscillator delay at a fixed leakage current is achieved (s. Fig. 9); The improvement on ring oscillator benefits from lower overall capacitance.

In addition, our eSiGe process maintains the very low leakage currents expected of a low power technology. PFET on-state gate leakage is kept below 10pA/μm while the off-state leakage is below 1pA/μm as shown in Fig. 10. Critical area and perimeter junction leakages are not degraded (s. Fig. 11) while the pFET GIDL current exhibits a significant 15X reduction due to implant optimization for retaining eSiGe strain (s Fig. 12).

Conclusion

Record high pFET performance is demonstrated by combining the various strain elements such as DSL and eSiGe in a low power 45nm bulk CMOS process. A significant reduction of the ring oscillator delay is achieved while maintaining very low leakage currents to satisfy the stringent requirements of portable wireless and multimedia devices.

Acknowledgement

This work was performed at the IBM Microelectronics, Div. Semiconductor Research & Development Center, Hopewell Junction, NY 12533. The authors would like to thank our colleagues for their support of this work.

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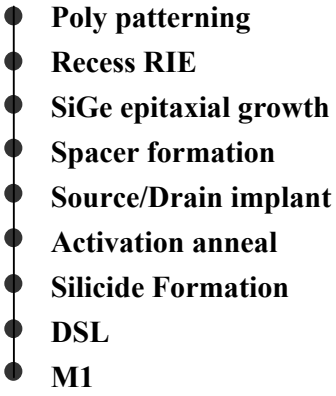

Fig 1: Process flow of pFET with eSiGe

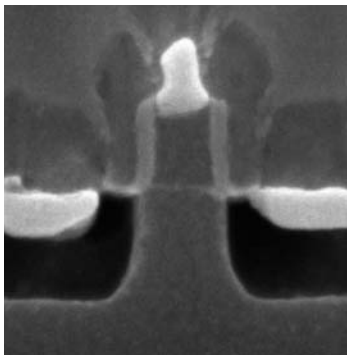

Fig 2: Cross sectional SEM of pFET with eSiGe

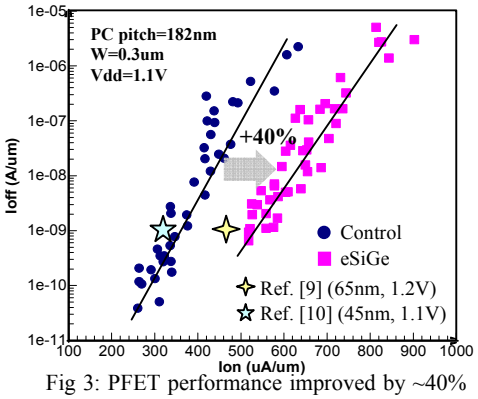

Fig 3: PFET performance improved by ~40% with eSiGe at Vdd=1.1V

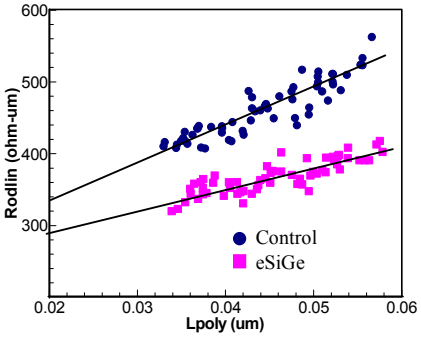

Fig. 4: PFET R_{ON} at fixed gate overdrive as a function of gate length showing short channel hole mobility enhancement with eSiGe.

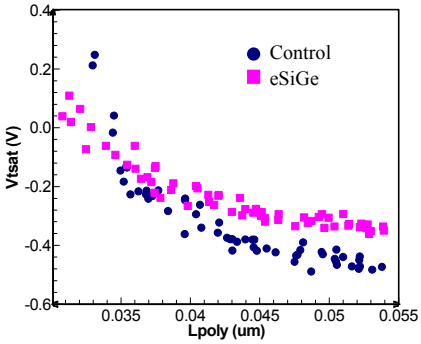

Fig 5: PFET Vtsat as a function of gate length showing improved rolloff performance.

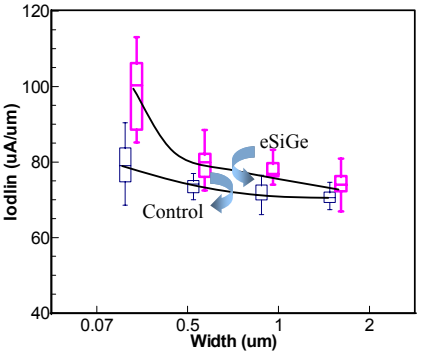

Fig.6: PFET linear current at fixed gate overdrive as a function of device width.

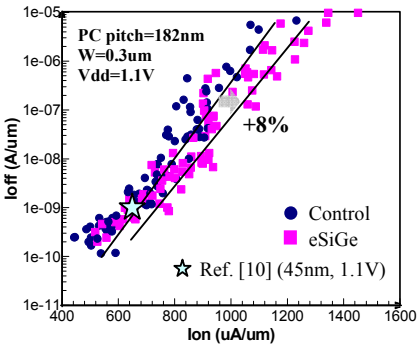

Fig 7: NFET performance enhanced by ~8% using eSiGe process flow.

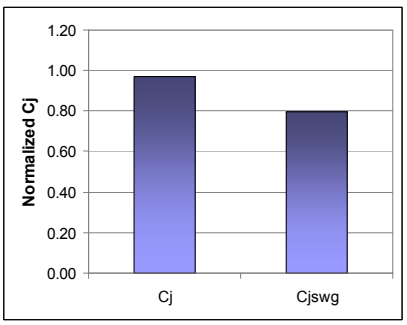

Fig. 8: Normalized p^+/NW area & sidewall junction capacitance with eSiGe

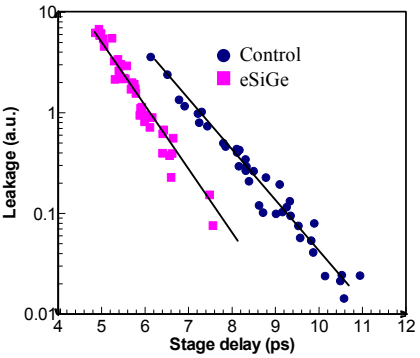

Fig.9: Ring oscillator stage delay vs. leakage current is reduced by ~25% with eSiGe

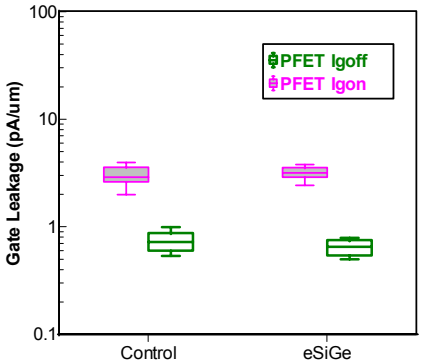

Fig. 10. Comparable pFET gate leakage obtained with eSiGe process

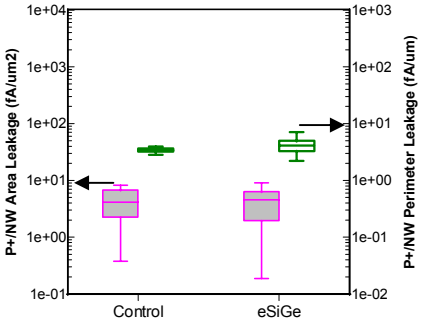

Fig. 11: Area & perimeter junction leakage as a function of process showing comparable performance

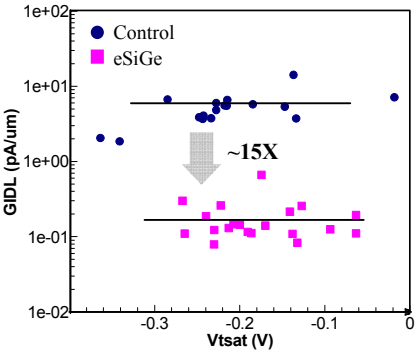

Fig. 12: PFET GIDL current as a function of Vtsat. 15X improvement obtained by eSiGe & implant optimization.