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In-Depth Study of Two-Dimensional Layout Dependences in Multiple-Stressor CMOS for 45 nm Technology Node High-Performance Applications

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Abstract

This paper describes the two-dimensional (2-D) layout dependences caused by dual stress liner (DSL) integration for 45 nm node high-performance (HP) devices with multiple-stressor technology (MST). It is demonstrated that both the lateral and transverse boundary positions significantly affect device characteristics such as threshold voltage and drive current, and these effects become much more pronounced in the devices with higher channel strains by MST. Based on these results, we developed new SPICE simulation procedure and made it possible to simulate various layout circuits accurately with taking into account 2-D DSL layout dependences.

Introduction

In order to break I_{on}-L_{min} trade-offs [1], in which drive current is rapidly decreased with the shrinkage of physical gate length below 40 nm regime, one of the most powerful methods is to use multiple-stressor technology (MST) [2-6], and it has thus been widely introduced not only into high-performance (HP) devices, but also into those of low operation power (LOP) and low standby power (LSTP). Indeed, dramatic carrier mobility enhancement and the resultant drive current improvement have been realized with MST; however, the issues of strain induced layout dependences have newly arisen [7], especially for small geometry devices. In this paper, we explore in-depth the impact of layout dependences on the CMOS device performance originated from the dual stress liner (DSL) scheme [8] in MST for the 45 nm technology node HP applications. We also discuss our strategy of MST and SPICE modeling by taking into account these layout dependences.

Multiple-Stressor Technology

Table I shows the summary of our MST used for the 45 nm technology node. Devices with standard <110> channels on (100) substrate were fabricated. For NFETs, poly gate stressor (PGS) and a tensile contact etching stop layer (tCESL) were adopted, whereas for PFETs, embedded SiGe (eSiGe) and compressive CESL (cCESL) were introduced as MST for both devices' performance enhancement. These technologies were integrated with the sequence as shown in Table I. The multiple stressors can be easily introduced into core logic circuit; however, they should be carefully selected for the SRAM to achieve high yield by minimizing the characteristic variations. Our strategy is that eSiGe, PGS, and DSL are not used and only the tCESL is introduced to both N and PFETs in SRAM to obtain a high read current by enhancing NFETs performance. Although DSL is indispensable technology, one of the concerns in DSL integration is contact opening at the DSL boundary. Fig.1 shows the distribution of gate contact resistance opened at the DSL boundary for various relative position relationships to the boundary. Even for the worst case where no CESL exists (corresponds to (e)), it is observed that the contact resistance is sufficiently low and well distributed compared with that of other relative contact positions. However, when the contact size is further scaled, the process difficulty increases and the open failure is observed as shown in Fig.2. We, therefore, prohibit laying out the contact at the DSL boundary in our design rule, although this brings about the requirement of a slightly relaxed layout.

Results and Discussion

Fig.3 shows the monitor layout for investigating the effect of the DSL boundary on the transistor characteristics used in this paper. Both the lateral and transverse DSL boundary positions are expressed with the parameters of SLL (gate edge to boundary) and SLW (active to boundary), respectively. SD diffusion lengths (L_{sd}) are fixed to 0.5 μm, therefore, the distance between active edge and boundary in the lateral direction is expressed by (SLL - 0.5) μm. In addition to the monitor with normal polarity (*e.g.*, tCESL over NFET), that of inverse polarity (cCESL over NFET) was evaluated for detailed understanding of strain dependences. In Fig.3, plan-view SEM photographs of these monitors just after the DSL module are also shown, and it is clear that they were successfully fabricated as we expected.

Figs.4 and 5 show the saturation V_t dependence on both SLL and SLW, respectively, for narrow and wide channel devices. Here, V_t is plotted for relatively long devices (L_g = 80 nm) in order to eliminate the short-channel effect (SCE) induced V_t variations. As for the lateral boundary effect, it is shown that V_t becomes deeper with the decrease of SLL for both N and PFETs. This is due to the decrease in strain induced subband splitting with the decrease of lateral channel strain as a result of closer lateral DSL boundary to the channel. In addition, the V_t shift is almost independent of channel width. For the transverse direction as shown in Fig.5, V_t's shift monotonically for NFETs; however, for PFETs, it once becomes shallow with the decrease of SLW then becomes deep below the 0.15 μm regime, and the V_t shift is much larger for narrow devices. This behavior indicates that transverse boundary effects are more complicated in which both the lateral and transverse channel strains are simultaneously changed. Although strain induced V_t shift is relatively large, its impact on V_t fluctuations is almost negligible as shown in Fig.6.

Next, we investigated the impact of the DSL boundary on the drive current. Fig.7 shows the relative NFET I_{on} as a function of SLL. It can be clearly seen that the I_{on} is decreased with decreasing SLL, and the worst I_{on} degradation by 12% was observed at SLL = 0.2 μm, where the boundary is located within the active region. Of course this I_{on} degradation is partly due to the V_t shift as shown previously, but the impact of mobility degradation with the reduced channel strain is predominant as shown in the inset I_{on}-I_{off} characteristics. Moreover, I_{on} dependence on SLL for the case of inverse polarity is almost symmetrical indicating that the ideally additive strain effects are introduced into the channel with MST. As for PFETs, on the other hand, the I_{on} dependence on SLL is similar to that of NFET, but the relative change of I_{on} is much larger as shown in Fig.8. This can be attributed to the larger Piezoresistance coefficients (π_l) of PFET [9] and larger intrinsic film stress in cCESL. Note that the device without eSiGe, that is, without elevated-SD is more sensitive to SLL. On the other hand, the transverse boundary effects on the drive current are shown in Figs.9 and 10. The major difference, when comparing with the lateral boundary effects, is larger channel width dependence, and it can be seen that the narrower the channel width, the more sensitive to SLW. In addition, PFET I_{on} dependence on SLW (Fig.10) is quite different compared to that of NFET (Fig.9). The PFET I_{on} increases with the decrease of SLW down to 0.15 μm, then rapidly decreases especially for the narrow device. Since both the lateral compressive and transverse tensile strains are effective for hole mobility enhancement, the decrease in SLW improves PFET I_{on}; however, lateral compressive strain is also decreased with further decreasing SLW, consequently, PFET I_{on} dependence shown in Fig.10 was observed. We also confirmed this behavior by 3-D process simulation (not shown). Figs.11 and 12 plot $\Delta I_{on}/I_{on}$ and $\Delta I_{dlin}/I_{dlin}$ correlation with varying SLL and SLW, respectively. In these figure, open symbols correspond to the devices having small SLL and SLW, where boundaries are located within the active region. Both the $\Delta I_{on}/I_{on}$ and $\Delta I_{dlin}/I_{dlin}$ are well correlated, but the I_{on} enhancement against the I_{dlin} enhancement is relatively large (larger slope in the figures) compared to the reported values with CESL [7].

In Fig.13, we compared the 2-D layout dependent I_{on} change for different channel strain devices with MST. NFET channel strain was changed by the thickness of tCESL and that of PFET was changed by the thickness of cCESL and Ge mole fraction in eSiGe. It is clear that higher channel strain devices show larger layout dependence for both N and PFETs. Even for allowable layout, I_{on} change by more than 10% is observed in high strained devices; therefore, it should be carefully taken into account these layout dependent performance changes for circuit design of multiple-stressor HP devices.

Finally, based on these results, 2-D DSL boundary effects were modeled with regression analysis and accounted for the BSIM4 model [10]. Fig.14 shows the procedure of SPICE simulation with taking into account the DSL boundary effects. By using three parameters related to mobility, threshold voltage, and saturation velocity, we can accurately simulate circuit performance with any layout of DSL boundary.

Conclusion

The effects of 2-D layout dependences caused by DSL integration were comprehensively investigated for 45 nm HP CMOS devices. It is clarified that the lateral boundary effects were simple and brings monotonic change in device performance; however, the transverse effects were complicated due to 2-D strain effects especially for narrow PFETs. These effects were accurately modeled and successfully taken into SPICE simulations.

Table I. Details of MST and its sequence of process integration for the 45 nm HP bulk devices.

Stressor	N or P	Core logic	I/O	SRAM
Embedded SiGe (eSiGe)	PFET	✓	-	-
Poly gate stressor (PGS)	NFET	✓	-	-
Tensile CESL (tCESL)	NFET	✓	✓	✓*
Compressive CESL (cCESL)	PFET	✓	✓	-

DSL

* No DSL

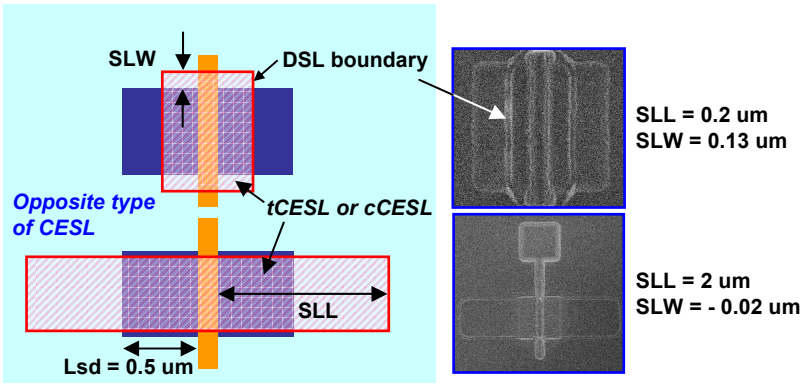


Fig.3. Monitor layout for characterizing the impact of the DSL boundary.

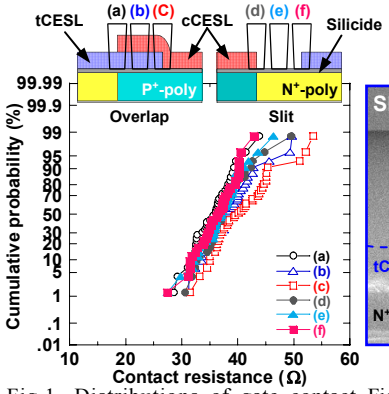


Fig.1. Distributions of gate contact resistance opened at the DSL boundary for different position relationships.

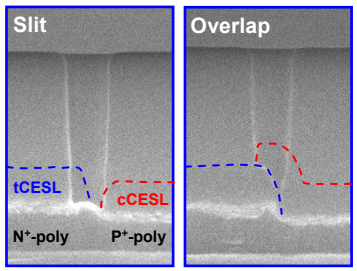


Fig.2. Cross-sectional SEM images of gate contact for scaled contact size at the DSL boundary.

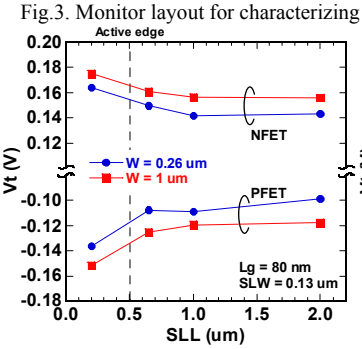


Fig.4. Saturation V_t dependence on the lateral DSL boundary position.

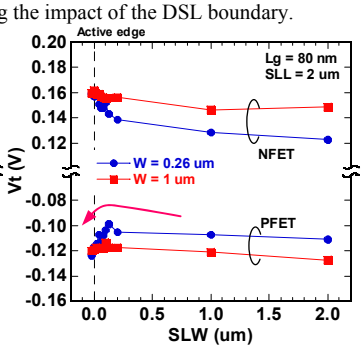


Fig.5. Saturation V_t dependence on the transverse DSL boundary position.

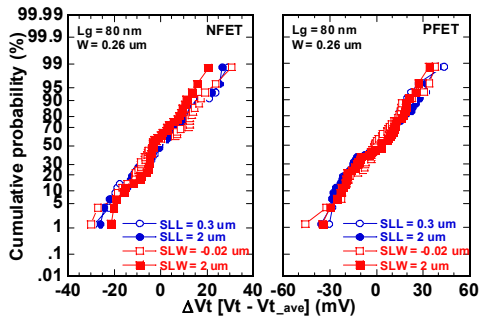


Fig.6. DSL boundary effect on V_t variation for both lateral and transverse directions.

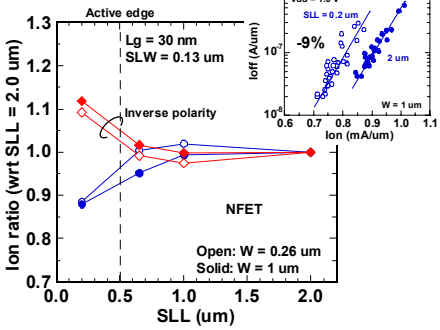


Fig.7. Relative NFET I_{on} as a function of SLL. Inset shows the I_{on}-I_{off} change for SLL = 0.2 and 2 μm.

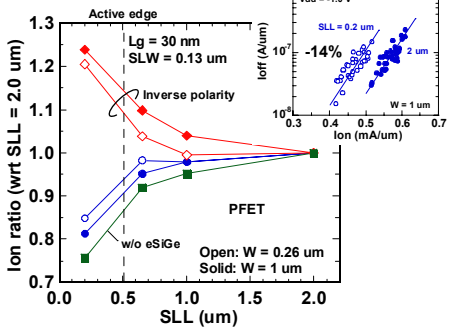


Fig.8. Relative PFET I_{on} as a function of SLL. Inset shows the I_{on}-I_{off} change for SLL = 0.2 and 2 μm.

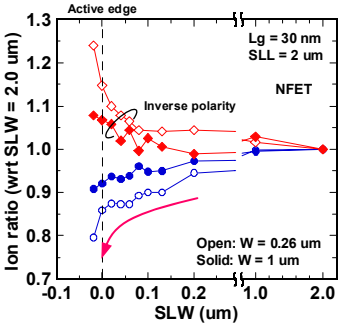


Fig.9. Relative NFET I_{on} as a function of SLW.

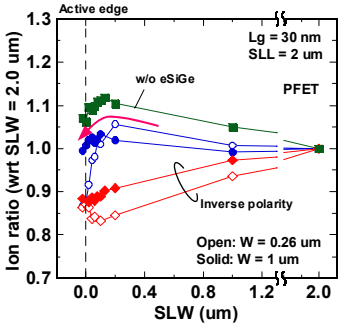


Fig.10. Relative PFET I_{on} as a function of SLW.

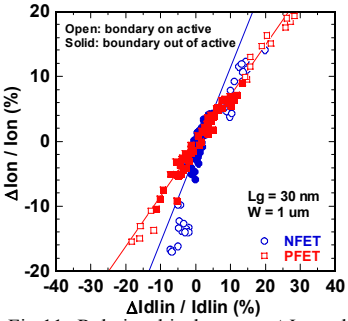


Fig.11. Relationship between ΔI_{on} and ΔI_{dlin} with varying lateral boundary.

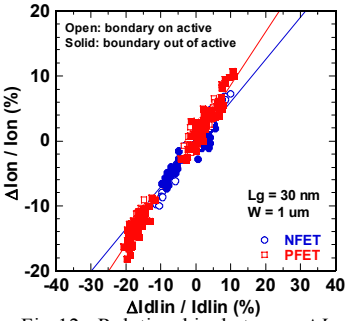
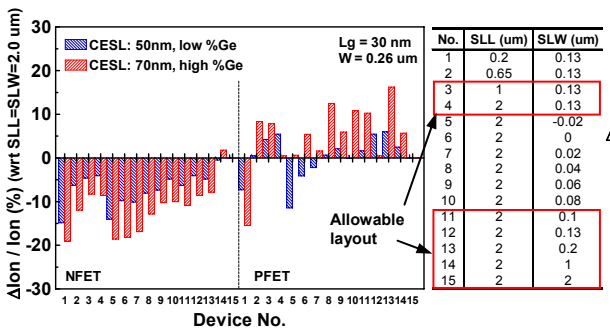


Fig.12. Relationship between ΔI_{on} and ΔI_{dlin} with varying transverse boundary.



No.	SLL (um)	SLW (um)
1	0.2	0.13
2	0.65	0.13
3	1	0.13
4	2	0.13
5	2	-0.02
6	2	0
7	2	0.02
8	2	0.04
9	2	0.06
10	2	0.08
11	2	0.1
12	2	0.13
13	2	0.2
14	2	1
15	2	2

Fig.13. I_{on} enhancement as a function of 2-D boundary position for different channel strain devices.

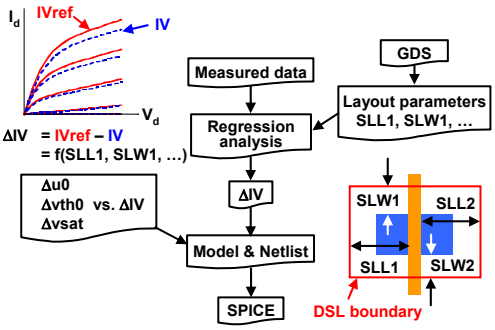


Fig.14. Procedure of SPICE simulation with taking into account 2-D boundary effects.

References

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