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Behavior of Low-Temperature Phonon-Limited Electron Mobility of Double-Gate Field-Effect Transistor with (111) Si Surface Channel

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1. Introduction

The phonon-limited electron mobility on the (001) Si surface of ultra-thin body (UTB) single-gate (SG) and double-gate (DG) SOI MOSFET's has been widely analyzed [1, 2], and its merits are well known. Recently, the electron mobility on the (110) Si surface of SG and DG SOI MOSFET's has been analyzed, and various strain techniques have been proposed and experimentally verified [3]. However, the results yielded by fabrication costs are high because strain device fabrication requires new fabrication processes and/or materials. We still think that another approach is needed to improve the performance of UTB DG SOI MOSFET's or FinFET's.

We have already demonstrated that the phonon-limited inversion-layer electron mobility of DG SOI MOSFET with a (111) Si surface at room temperature is superior to that of SG SOI MOSFET when SOI layer thickness is around 5 nm [4] with the aid of 1-D self-consistent calculations and relaxation time approximations [5, 6].

In this paper, electron mobility behaviors on the (111) and (001) Si surface of DG SOI MOSFET at low temperature is analyzed [2]. We examine whether the phonon-limited inversion-layer electron mobility of DG SOI MOSFET with the (111) surface at low temperature is still much superior to that of SG SOI MOSFET.

2. Device structure and simulations

The simulations assume SG and DG n-channel SOI MOSFET's. It is further assumed that the gate oxide thickness (T_{ox}) of the SG and DG SOI MOSFET's is 3 nm and the buried oxide layer thickness (T_{BOX}) of the SG SOI MOSFET is 200 nm. Impurity concentrations (N_A) in the SOI-layer and Si substrate are taken to be 5×10^{15} cm^{-3} [4].

This study simulates the phonon-limited electron mobility in the inversion layers of SG and DG SOI MOSFET's on (111) and (001) Si surfaces at low temperature using a relaxation time approximation based on a 1-D self-consistent simulations [5, 6].

3. Results and Discussions

Simulated phonon-limited electron mobility on the (111) Si surface at 300 K is shown in Fig. 1 as a function of E_{eff}. The electron mobility of DG FET with 6-nm T_{SOI} exceeds that with 30-nm T_{SOI} for E_{eff} > 0.5 MV/cm; in contrast, the SG FET does not exhibit such behavior [4]. Simulated phonon-limited electron mobility on the (111) surface at 77 K is shown in Fig. 2 as a function of T_{SOI} for various E_{eff} values; simulated mobility values of the DG and SG FET's are compared. It is seen that the DG SOI MOSFET having T_{SOI} values ranging from 5 to 15 nm offers a superior mobility for medium and high E_{eff} values. In particular, the maximal mobility enhancement is expected around T_{SOI} = 6 nm for E_{eff} > 0.5 MVcm^{-1}.

Low-temperature behaviors of phonon-limited electron mobility on the (111) Si surface and (001) Si surface are shown as a function of E_{eff} for DG and SG FET's in Fig. 3 and Fig. 4; respectively. The electron mobility on the (111) Si surface of the DG FET with a 6-nm T_{SOI} exceeds that with 30-nm T_{SOI} for E_{eff} > 0.3 MV/cm (see Fig. 3); in contrast, the SG FET does not exhibit such behavior. As shown in Fig. 3, the DG FET with a 6-nm T_{SOI} has a higher electron mobility than the SG FET for E_{eff} > 0.2 MVcm^{-1}. These results are very interesting because they are not seen in SOI MOSFET's with (001) Si surfaces for medium and high E_{eff} values (see Fig. 4) [2].

The expected phonon-limited electron mobility of a 6-nm T_{SOI} DG FET with (111) Si surfaces is 4635 cm^{2}V^{-1}s^{-1} at E_{eff} = 1 MVcm^{-1}; this is 98 % of that of the equivalent DG FET with (001) Si surfaces, which is quite interesting from the viewpoint of low-temperature device applications [7].

In Fig. 5, low-temperature phonon-limited electron mobility of lowest-subband electrons (m_0) versus E_{eff} is shown for 6-nm-T_{SOI} DG and SG FET's; for the lowest-subband electrons, acoustic-phonon-limited mobility ($m_{0,intra}$) and optical-phonon-limited mobility ($m_{0,inter}$) are also shown separately. Fig. 5 suggests that optical-phonon scattering of the lowest-subband electrons of 6-nm-T_{SOI} devices is not suppressed in a high E_{eff} range, but that acoustic-phonon scattering is well suppressed in a medium E_{eff} range at 77 K.

Figure 6 plots E_{eff} dependencies of occupation fractions of electrons sharing the lowest subband (f_0) and the 2nd subband (f_1) for 6-nm T_{SOI} SG and DG FET's; form factors (F_{ij}) of electrons are also shown for comparison because the form factor (F_{ij}) influences the probability of transition from the subband i to j. Acoustic-phonon scattering of the lowest-subband electrons is well suppressed at medium E_{eff} values for the 6-nm-T_{SOI} DG FET, while it isn't suppressed at high E_{eff} values as seen in Fig. 5. The F_{00} value of the 6-nm-T_{SOI} DG FET decreases as E_{eff} increases, which results in the suppression of acoustic-phonon scattering of the lowest-subband electrons; however, the suppression of acoustic-phonon scattering becomes modest at high E_{eff} values because the decrease in subband-to-subband energy difference promotes the transition between the lowest subband and the 2nd subband as is anticipated from the increase in F_{01} at high E_{eff} values [1].

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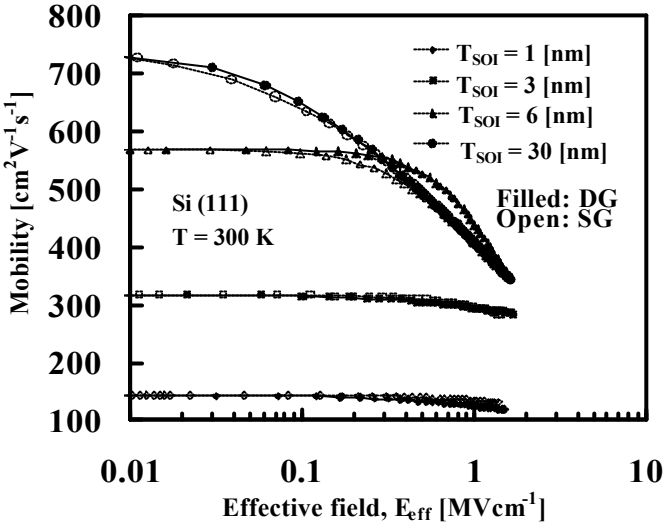

Fig. 1. E_{eff} dependencies of phonon-limited electron mobility on the (111) Si surface at 300 K as a parameter of T_{SOI}.

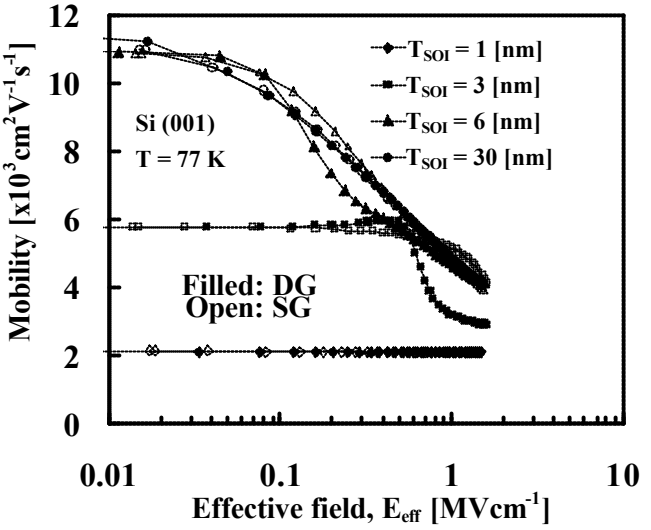

Fig. 4. E_{eff} dependencies of phonon-limited electron mobility on the (001) Si surface at 77 as a parameter of T_{SOI}.

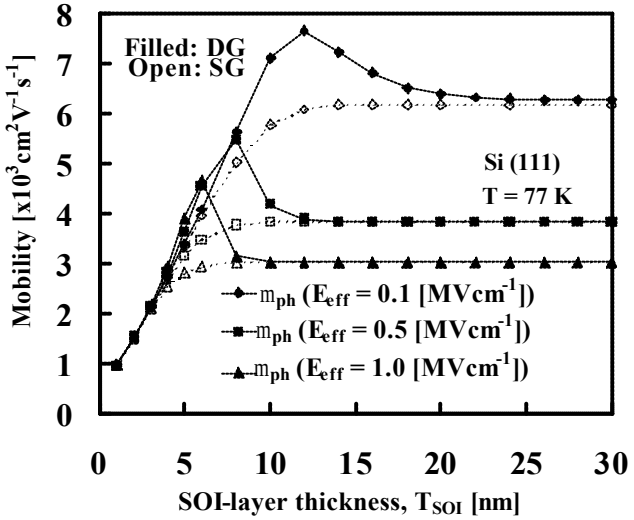

Fig. 2. T_{SOI} dependencies of phonon-limited electron mobility on the (111) Si surface at 77 as a parameter of E_{eff}.

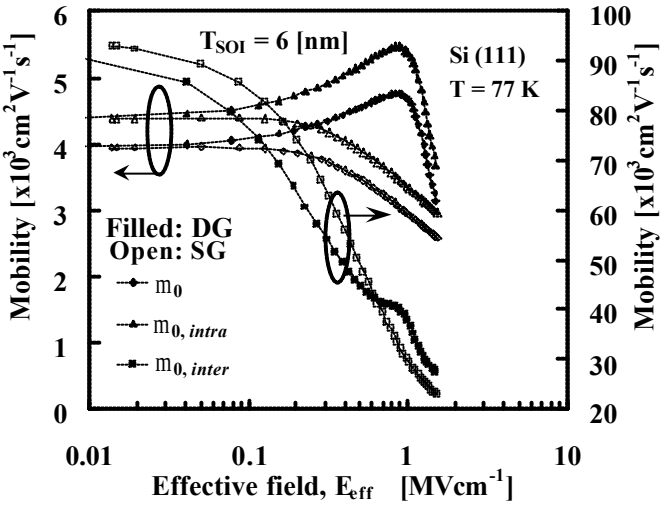

Fig. 5. E_{eff} dependencies of lowest-subband phonon-limited electron mobility are shown. Acoustic-phonon-scattering-limited mobility, $m_{0,intra}$, and optical-phonon-scattering-limited mobility, $m_{0,inter}$, are shown separately for SG and DG SOI MOSFET with (111) Si surface channel; m_0 is overall mobility including $m_{0,intra}$ and $m_{0,inter}$.

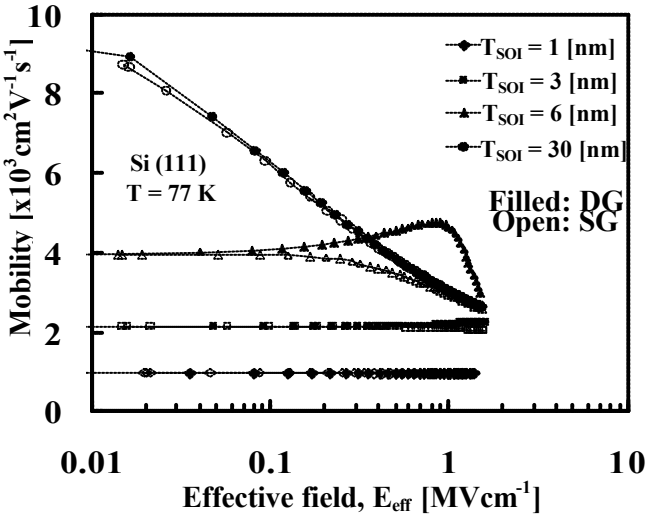

Fig. 3. E_{eff} dependencies of phonon-limited electron mobility on the (111) Si surface at 77 K as a parameter of T_{SOI}.

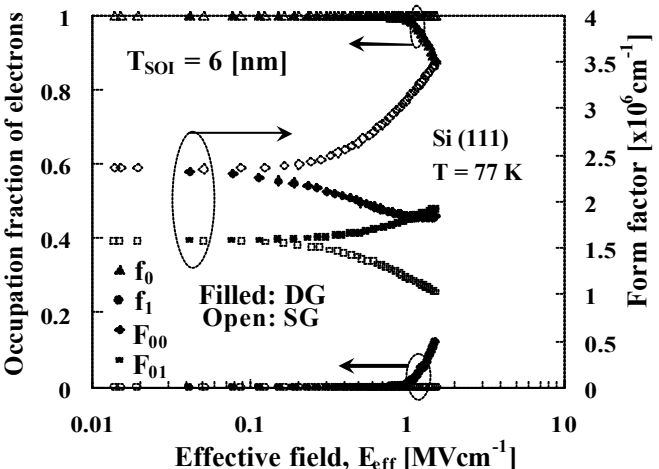

Fig. 6. E_{eff} dependencies of occupation fractions of electrons sharing the lowest subband for 6-nm-T_{SOI} SG and DG FET's. Respective form factors are also shown for comparison at 77 K.