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Mobility Degradation in (110)-Oriented Ultra-thin Body Double-Gate pMOSFETs with SOI Thickness of less than 5nm

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Abstract

Mobility degradation in (110) oriented ultra-thin body double-gate pMOSFETs was experimentally observed for the first time. The reason of this degradation is discussed in terms of the carrier repopulation.

1. Introduction

Much attention has been paid on (110)-oriented MOSFETs because of its superior hole mobility to the conventional (100) surface [1]. Recent works have demonstrated that (110) surface MOSFETs show better performance even if their SOI thickness (t_{SOI}) is thinned ultimately [2,3], since their mobility is enhanced by suppression of phonon scattering when t_{SOI} is around 3-4 nm. However, these measurements have been made in the single-gate operation and few works have been done on the performance of (110) Ultra-thin Body (UTB) pMOSFETs in the double-gate operation. Note that the main current path in a FinFET, one of the promising double-gate structures, is (110) surface if it is fabricated on conventional (100) substrate. Thus, it is quite necessary to understand the mobility behavior in (110)-oriented pMOSFETs in double gate operation.

In this paper, the effective mobility (μ_{eff}) of (110)-oriented UTB pMOSFETs was experimentally evaluated and severe mobility degradation was observed in double gate operation compared to single gate operation for the first time. The possible mechanism of the mobility degradation is discussed.

2. Device fabrication and Experiments

The devices used in this study were fabricated on a (110)-oriented UNIBOND SOI wafer. Both the gate length and width are 200 μm. The gate oxide thickness is about 17 nm and the buried oxide thickness is about 145 nm. A schematic device structure is shown in Fig. 1. The source/drain region is kept thicker using the LOCOS technique to make the parasitic resistance negligible [2]. t_{SOI} was estimated by the spectroscopic ellipsometry.

Mobility was extracted experimentally by split C-V method at room temperature. In the double-gate operation, the backgate bias (V_b) was applied so that the inversion charge is twice as much as that at V_b = 0 V [4].

3. Results

Fig. 2 shows the C_g-V_g characteristics of (110) UTB pMOSFETs. As t_{SOI} becomes thinner, V_{th} shifts and the capacitance increases, which are caused by the quantum mechanical effect in the ultimately thin t_{SOI} [5]. Although t_{SOI} was estimated with the spectroscopic ellipsometry, the relative thickness of each device is in good agreement with the Vth shift shown in Fig. 2.

Fig. 3 compares the μ_{eff}–N_{inv} characteristics in single-gate and double-gate operations when t_{SOI} is relatively thick. N_{inv} of double-gate are taken as half of N_{inv} of single-gate [4]. When t_{SOI} is thicker than 5.1 nm, μ_{eff} in the double-gate operation is almost the same as that of the single-gate operation at high N_{inv} (around 10^{13} cm^{-2}). Thus, the volume inversion at high N_{inv} region, which has been observed in UTB nMOSFETs [3], is not observed in UTB pMOSFETs, and these results are consistent with a previous report [3].

Fig. 4 compares the μ_{eff}–N_{inv} characteristics in single-gate and double-gate operations when t_{SOI} is ultimately thin. To show the mobility behavior in more detail, mobility comparison at N_{inv}=1.0x10^{13} cm^{-2} with different t_{SOI} are shown in Fig. 5. The mobility enhancement is clearly observed when t_{SOI} is 3.6 nm due to the suppression of phonon scattering as reported in [3], and the mobility degradation in both single-gate and double-gate operations is observed when is t_{SOI} 1.8 nm possibly due to the δ-t_{SOI} induced scattering [5].

A new finding in this study is that the clear mobility degradations (compared to single-gate operation) are observed at high N_{inv} in the double-gate operation when t_{SOI} is thinner than 3.6 nm. To our knowledge, this is the first experimental demonstration of mobility degradation in (110)-oriented UTB pMOSFETs in the double-gate operation.

4. Discussions

Similar phenomena of the mobility degradation in double gate operation have been reported in (100) UTB nMOSFETs [5], and it was explained in terms of δ-t_{SOI} induced scattering mechanism. Generally, the mobility limited by δ-t_{SOI} induced scattering ($\mu_{\delta\text{-}tSOI}$) is proportional to $(m_z/m^*)^2$ [6]. Thus, if the population of the subband with heavier conductivity mass increases, the δ-t_{SOI} induced scattering also increases, resulting in mobility degradation. It is well-known that the holes in (110) surface are highly degenerated [7] and m_z is larger than that of 2-fold valley in the (100) conduction band [8]. Thus, it is speculated that the hole populations in (110) UTB pMOSFETs are different in the single-gate and double-gate operations and that the double-gate operation has more holes in the band with heavier m_z, resulting in the mobility degradation.

5. Conclusions

Mobility degradation in (110) UTB pMOSFETs in double gate operation was demonstrated for the first time.

In terms of the effective mobility, (110) oriented UTB pMOSFETs with t_{SOI} less than 5 nm should not be operated in double gate to obtain sufficient quantum-mechanical benefits in UTB scheme.

s s Reference

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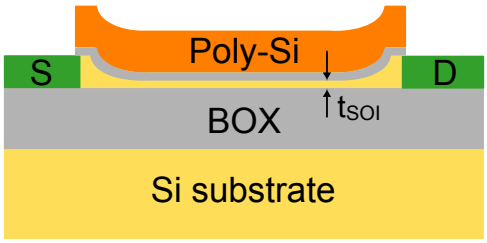

Fig.1 A schematic diagram of fabricated devices. Note that source / drain region was kept thicker to minimize the parasitic resistance.

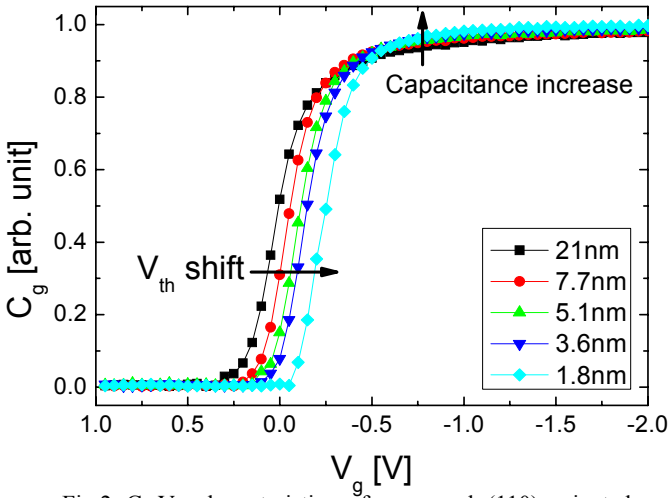

Fig.2 C_g-V_g characteristics of measured (110) oriented UTB pMOSFETs. V_{th} shift and capacitance increase were observed due to the t_{SOI} confinement. From these facts, relative t_{SOI} estimation is appropriate.

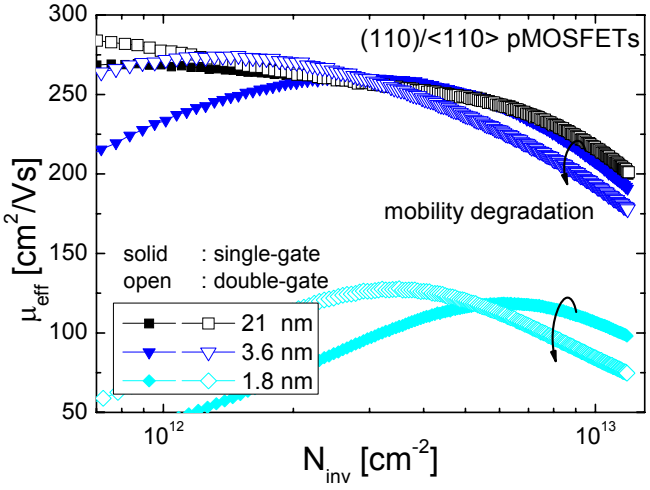

Fig.4 μ_{eff}–N_{inv} characteristics of (110) oriented UTB pMOSFETs in single- and double-gate operation with different t_{SOI}. The mobility of 21 nm device is the same one as shown in Fig. 3. Severe mobility degradations were observed when t_{SOI} is less than 3.6 nm.

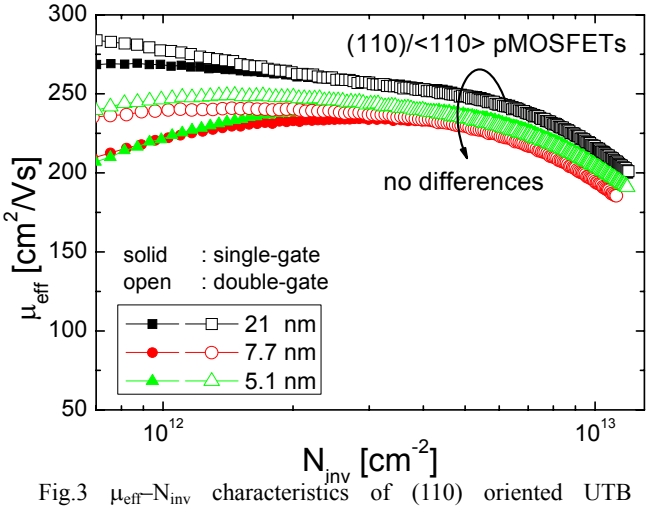

Fig.3 μ_{eff}–N_{inv} characteristics of (110) oriented UTB pMOSFETs in single- and double-gate operation with different t_{SOI}. Mobility difference between single and double gate operation is not observed when t_{SOI} is more than 5.1 nm. These results are consistent with a previous report [2], indicating the validity of our measurement method.

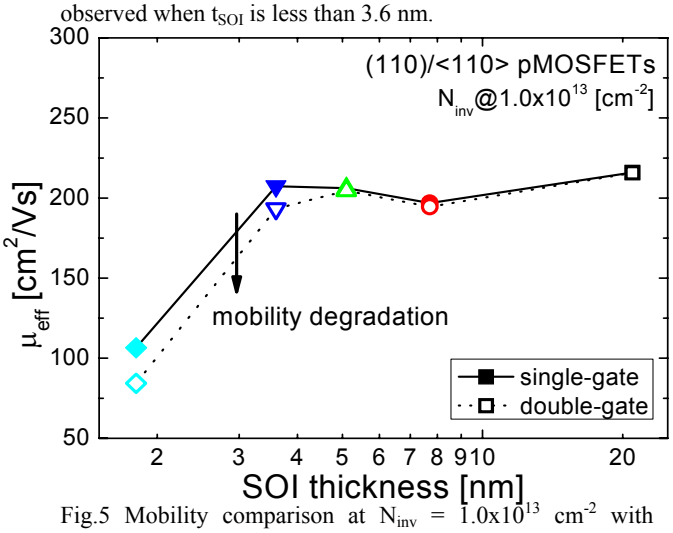

Fig.5 Mobility comparison at N_{inv} = 1.0x10^{13} cm^{-2} with different t_{SOI}. As mentioned above, mobility degradation at high N_{inv} is observed.