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Device Performance and Reliability Considerations of Biaxially Strained Si by Wafer-Bonding-Technology

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Abstract— Biaxial tensile-strain (~0.012% to ~0.04%) is realized on Si wafer using novel thermal bonding technique with flame retardant (FR4) material of different thicknesses. Numerical modeling using 3D finite element analysis show strain of up to 0.04% can be achieved using this technique with drive current improvement of up to 11% on n-MOSFET and 8% for p-MOSFET. Strained samples shows gate leakage reduction (increase) in n- (p-) MOSFET by up to 7% due to strain-induced barrier height lowering. Reliability studies on post-backend biaxial tensile-strained nMOSFETs show enhanced oxide-charge-trapping but in-significant degradation at SiO_2/Si interface under constant-voltage-stress (CVS). Strained n-MOSFET devices also show enhanced impact ionization with shorter T_{BD} but tighter distribution of Weibull slope β.

I. INTRODUCTION

Strained silicon devices and their reliability have attracted much interest as the scaling of CMOS transistors progresses into the nanometer regime [1-6]. Most of these reliability studies have focused predominantly on heterostructure strained Si/SiGe which may be affected by the underlying SiGe [1]. Hot carrier and NBTI studies on strained (100) Si substrate (on relaxed SiGe buffer), show higher degradation due to enhanced lateral field [2], enhanced impact ionization arising from severe self-heating and positive temperature dependence [3]. Fischetti *et al.,* showed that the larger threshold voltage shift in biaxially strained silicon can be attributed to the strain-induced shift in the electron affinity and bandgap narrowing effect [4]. Recently, post-backend mechanical strain using either mechanical stress [5, 6] or wafer-bonding [7-9] have been demonstrated. Key advantage is the simplicity in processing and cost without the process complication of incorporating Ge. ***This study examines the effect of substrate strain on device characteristics of CMOS transistors and their reliability. As far as we are aware, this is the first time, the effects of externally-applied biaxial tensile strain on interface trap generation, oxide charge trapping and oxide breakdown for nMOSFETs have been reported.***

II. EXPERIMENTAL

CMOS transistors were fabricated on 8'' p-type Si (100) wafer (8-10 Ω-cm) using standard CMOS-0.13 µm processing with gate stack consisting of ~30Å SiO_2/PolySi. The completed wafers were thinned down to 200 µm, electrically characterized and bonded onto FR-4 (fire-retardant material) at 160˚C. Due to the difference in thermal expansion coefficients between the FR-4 material (15 ppm/˚C) and silicon and shrinkage of the bonding adhesive, the 8'' silicon wafer experienced a biaxial tensile-strain across the whole wafer. Finite element 3D modeling (ANSYS) shows a resultant strain of 0.012%, 0.034% and 0.040% for bond material thickness of 800µm, 250µm and 100µm respectively as shown in **Fig. 1.** Control devices refer to fresh devices on un-bonded silicon wafers while the strained devices refer to samples bonded to FR4 with a resultant biaxial tensile strain across the device.

III. RESULTS AND DISCUSSION

Figures 2 and 3 show drain current enhancement of n- and p-MOS transistor before and after substrate bonding (ε=0.04%). nMOSFET I_{dsat} and mobility enhancement (~11% at ε ≈ 0.040%) increase with biaxial strain while enhancement for p-MOSFETs is only significant at larger biaxial strain (~4% and ~8% at ε ≈ 0.034% and 0.040%, respectively). Insignificant changes in subthreshold slope, C-V characteristics (not shown) and V_T roll-off (**Fig. 4**) after FR4 bonding demonstrates a production worthy process. **Figure 5** shows the change in gate leakage current after substrate bonding with linear dependence on strain due to reduced hole and electron current in p- and n-MOSFET respectively (as verified by carrier separation). This can be attributed to strain induced changes in barrier height and out-of-plane mass [10]. Electrical degradation under constant voltage stress CVS is examined under both $\pm V_g$ bias. **Figures 6,7** show the gated diode measurement on the FR4 bonded samples along with control after +CVS(V_g=4V/time=10^3s). Strained samples show insignificant increase in interface traps generation under CVS but notable increase in negative charge trapping (positive shift in $V_{B,peak}$) in the oxide under +CVS. This is in contrast to uniaxial strain which has negligible change in both N_{OT} and N_{IT} generation [5]. Enhanced oxide charge trapping for strained devices is also reflected in V_T shift (**Fig. 8**) and the stress-induced leakage current (SILC) (**Figs. 9/10**) as $\Delta J_g / J_{g,0} = AQ^m$ [11] where A is the initial trap density and m is the generation rate constant and Q is the injected fluence. **Fig. 10** shows that enhanced SILC in strained samples can be modeled by an additional leakage path with rate constant m=~0.17(-CVS) and ~0.36(+CVS) and higher initial trap density A (proportional to the strain). Our results show that strain-induced degradation is more severe under positive CVS with significant increase in the oxide trapped charge but not in interface traps. In contrast, -CVS results in smaller degradation rate for strained samples (**Fig. 10 inset**). Under +CVS, conduction and valence electrons are injected from the substrate while holes are injected from the gate side. For -CVS, only holes are injected from the substrate. The key differences between –CVS and +CVS suggest that conduction electron under +CVS increases significantly under substrate strain. **Fig. 11** shows the substrate hole current under different gate bias with increased impact ionization for strained devices. This is consistent with bandgap narrowing in the channel and the offset is mainly in the conduction band, resulting in enhanced electron trapping (**Figs. 6, 10**). Due to enhanced defect generation, the Weibull plot for charge-to-BD and time-to-BD, has smaller Q_{BD} and T_{BD} values with higher Weibull slope β, consistent with enhanced electron trapping in strained devices .

IV. CONCLUSION

We have demonstrated post-processing wafer bonding technology with I_D-improvement of 11% on n- and 8% for p-MOSFETs. Oxide reliability for strained CMOSFET using wafer bonding technology shows enhanced impact-ionization due to bandgap narrowing with barrier lowering for electron, causing enhanced N_{OT} under +CVS but no degradation to interface traps.

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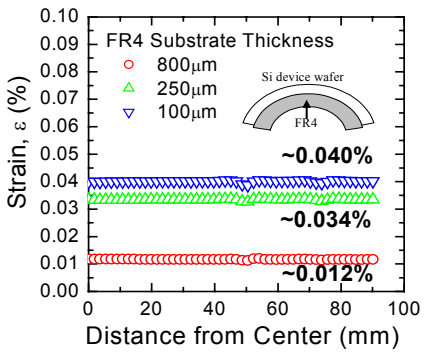

Fig.1 ANSYS simulation of lattice Si in-plane strain when thermally bonded to FR4 substrate with different thickness.

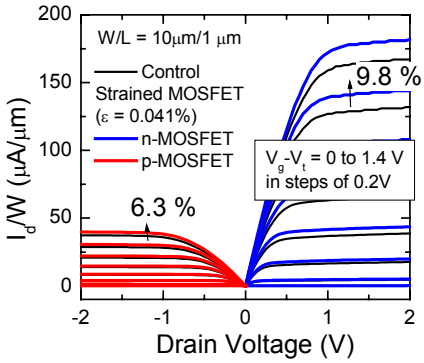

Fig.2 I_d-V_d characteristics of n/p-MOS before (control) and after substrate bonding. I_D improves by 9.8% and 6.3% for n-MOS and p-MOS respectively with ε = 0.04%.

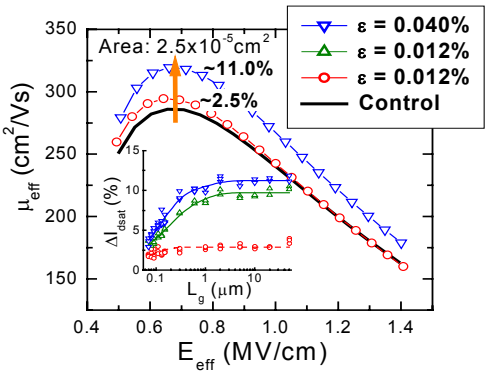

Fig.3 Electron mobility enhancement after FR4 thermal bonding. μ_{eff} is extracted from split C-V method for L_g = 10 μm. Inset shows I_{dsat} enhancement for different L_g with different FR4 thickness

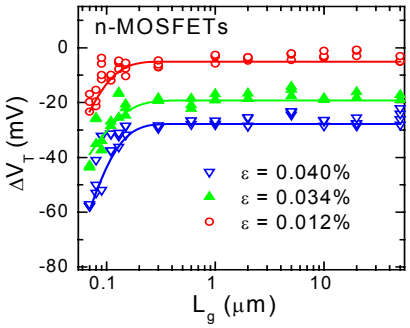

Fig. 4 Threshold voltage shift ($\Delta V_T = V_{T,stress} - V_{T,0}$) for n-MOSFET with different gate length under different substrate strain.

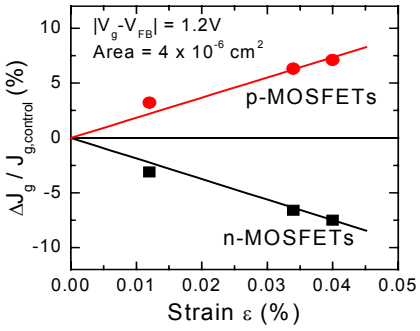

Fig.5 Strain-induced leakage current for n-MOS and p-MOS, measured under inversion mode. Carrier separation shows reduced (increased) Jg in nMOS(pMOS) due to reduced electron (increased hole) $J_{S/D}$. Results similar to [10]

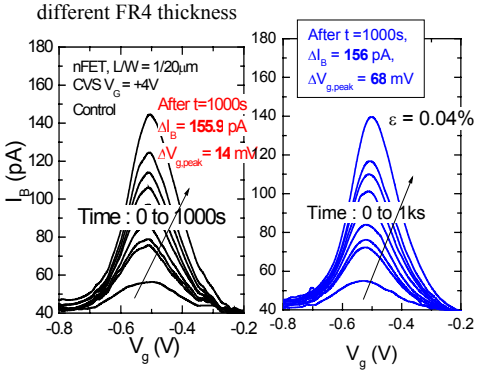

Fig.6 DCIV spectra for un-strained Si and substrate strained Si n-MOSFET (ε = 0.04%). Post-stressed base peak current $I_{B,peak}$ do not show significant changes for control and strained Si nMOSFET

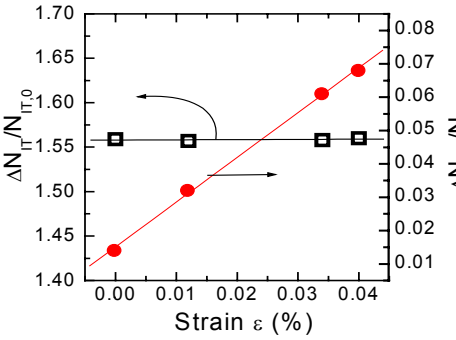

Fig.7 Change in $I_{B,peak}$ and $V_{g,peak}$ for different substrate strain after constant CVS (V_g = +4V) for time period of 1000s.

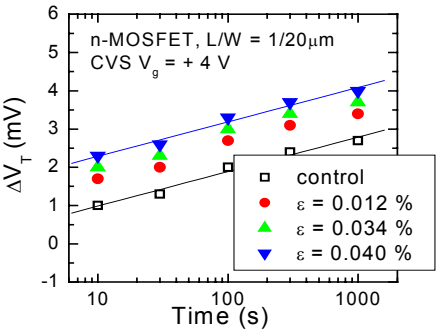

Fig.8 Evolution of threshold voltage change for different substrate strain.

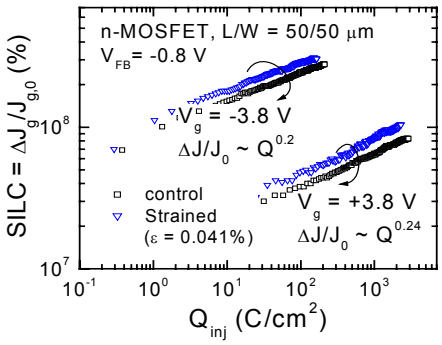

Fig.9 Stress-induced leakage current (SILC) for both strained and un-strained (control) samples under CVS (V_g = + 3.8 V and -3.8 V)

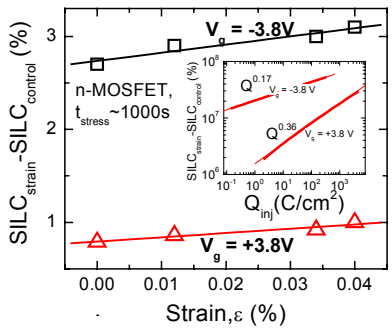

Fig.10 Comparison of SILC for strained and un-strained(control) samples as a function of substrate lattice strain under + and –CVS. Strained samples shows enhanced SILC which has an additional component with rate const m = 0.17 (-CVS), 0.36 (+CVS).

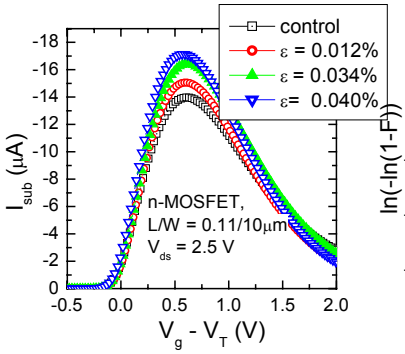

Fig.11 Substrate hole current for different strain. Enhanced lattice strain results in higher hole current, showing enhanced impact ionization.

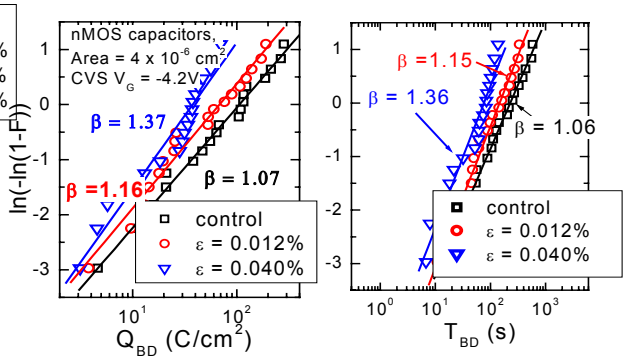

Fig.12 Weibull distribution of charge-to-breakdown Q_{BD} and time-to-breakdown T_{BD} for strained and un-strained (control) samples. Negative CVS (V_g = -4.2V) is applied with strained devices showing a shorter T_{BD} but higher β.