Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 738-739

B-6-3

LDMOS Model for Device and Circuit Optimization

M. Yokomichi, M. Miyake, T. Kajiwara, N. Sadachika, A. Yumisaki, H.J. Mattausch, M. Miura-Mattausch
Hiroshima University, 1-3-1 Kagamiyama, Higashi-Hiroshima, 739-8530, Japan
e-mail: m062926@hiroshima-u.ac.jp

1.Introduction

LDMOS devices are used in many automotive and mobile applications for high voltage switching. Requirements range from a few volts to several hundred volts. This wide range of the operation conditions is realized with the help of a low impurity concentration region, called drift region as shown in Fig. 1 [1]. It has been observed that the capacitance of any LDMOS device shows anomalous characteristics as a function of applied voltages, which are not yet modeled in a consistent way. Therefore, a good compact model covering all possible LDMOS structures is desired.

We have developed a compact LDMOS model called HiSIM-LDMOS. With this model it is verified, for the first time, how the transconductance g_m characteristics of the LDMOS device correlates with the anomalous behavior of the gate capacitance C_{gg} and the structure of the drift region and influence on switching performance.

2.Characteristics of the LDMOS device

Figs. 2a,b show simulated *I-V* and g_m characteristics with a 2D-device simulator. The results are obtained by varying the impurity concentrations in the drift region N_{drift}, while keeping the length L_{drift} and other model parameters the same. Corresponding C_{gg} are shown in Fig. 2c. Anomalies are observed with reduced N_{drift}, and a clear correlation between g_m and C_{gg} is seen. When g_m reduces abruptly with increased V_{gs}, anomalies in C_{gg} occur. Usually the channel region is fabricated by out-diffusion from the source. It is believed that the C_{gg} anomalies are caused by the gradient of the channel impurity concentration due to the out diffusion [2]. We find, however, that the impurity gradient affects the g_m characteristics in the same way as a reduction of N_{drift}, as verified in Fig. 3.

The abrupt reduction of g_m and the anomalies in C_{gg} are both caused by the resistance effect in the drift region. Thus the key for a good compact model is the accurate modeling of the resistance effect in the LDMOS.

3.Modeling approach

For modeling the resistance effect of the drift region in a consistent way, we have extended the bulk MOSFET model HiSIM, which solves the Poisson equation for surface potential values iteratively. In the iteration the resistance effect is included as the potential drop written

$$\Delta V = I_{ds} * R_{drift} \quad (1)$$

solved again by iteration as shown in Fig.4, where R_{drift} is the resistance in the drift region. In comparison to the bulk MOSFET, two additional charges are induced in the drift region for the LDMOS case. One is the overlap charge Q_{over} caused by formation of the accumulation as well as the depletion and the inversion condition underneath the gate overlap region. The second charge consists of the integrated carrier in the drift region, which is modeled with the drain current I_{ds}(= $n\mu E$). The electric field E is replaced with that in the drift region modeled as

$$E = (V_{ds} + V_{bi} - \phi_{sdl}) / L_{drift} \quad (2)$$

where ϕ_{sdl} is the potential value at the substrate/drift junction calculated. All these charges are calculated with the surface potential distribution shown in Fig. 5.

4.Verification of the developed model

Fig. 6 shows a comparison of model results for the V_{ds}=9V case. The high resistance in the drift region prevents current injection. This causes the abrupt reduction of g_m, and stops further charge increase in L_{drift} resulting in the anomalous spike for C_{gg}. The C_{gg} spike is further enhanced by higher driving capability of the channel with the impurity gradient as shown in Fig. 3. The C_{gg} anomaly degrades circuit performances drastically as demonstrated in Fig. 7. Therefore, the balance between the channel impurity concentration, determining the channel driving capability, and N_{drift} determining the resistance effect in L_{drift} has to be optimized for avoiding the C_{gg} anomalies.

5.Conclutions

We have developed a compact model for LDMOS based on the surface potential distribution in the MOSFET and its extension to the drift region. The model solves the entire LDMOS structure in a consistent way, reproducing structure-dependent device features and circuit performances based on these features.

Acknowledgements

We would like to express our sincere thanks to STARC for support and cooperation.

References

[1] C.Y. Tsai et al., Tech. Digest IEDM, p.367, 1997.
[2] Y.S. Chauhan et al., Tech. Digest IEDM, p.213, 2006.

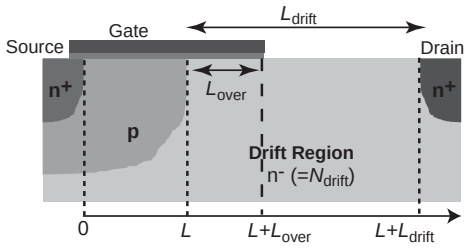

Fig. 1. Cross-section of the studied LDMOS

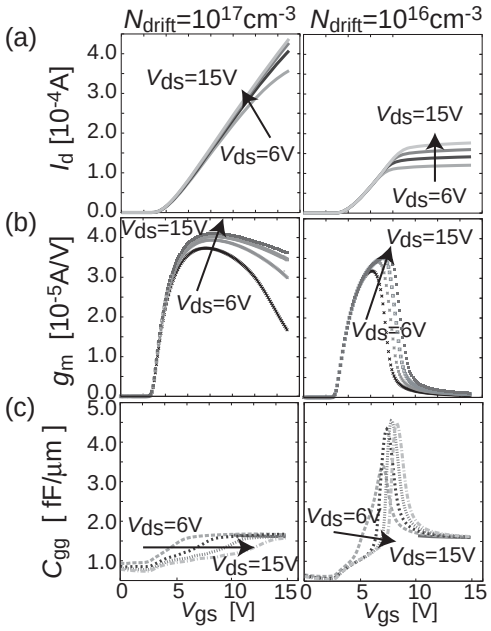

Fig.2. Comparison of simulated drain current, transconductance, and gate capacitance for two impurity concentrations in the drift region with a 2D-device simulator**.**

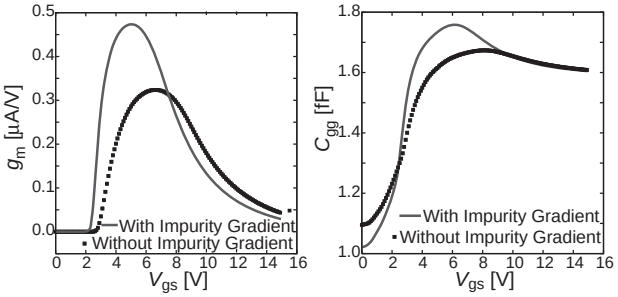

Fig.3. Comparison of simulated g_m and C_{gg} with (solid line) and without (dotted line) the impurity gradient of the substrate.

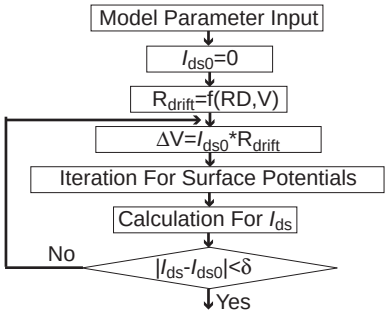

Fig. 4. Calculation flow chart of the LDMOS

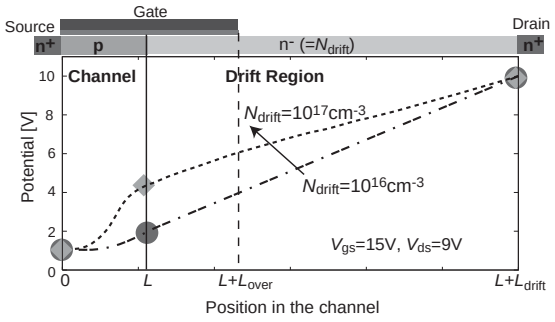

Fig. 5. Calculated potential distribution along the channel with the developed compact LDMOS model (shown with symbols) for two N_{drift} concentrations**.**

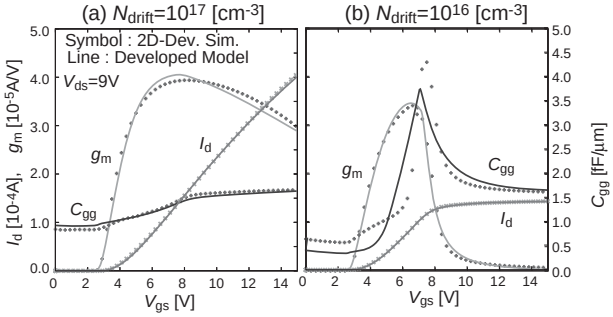

Fig. 6. Verification of the developed LDMOS model with 2D-device simulation results (a) for N_{drift}=10^{17}cm^{-3} and (b) for N_{drift}=10^{16}cm^{-3}.

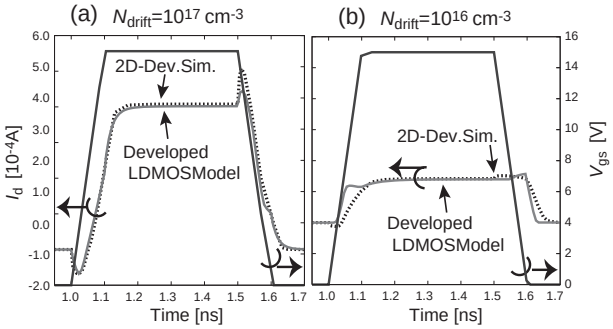

Fig.7.Calculated switching characteristics (a) for N_{drift}=10^{17}cm^{-3} and (b) for N_{drift}=10^{16}cm^{-3}. Clear degradation of the switching performance is seen for the (b) case.