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NMOS Current Enhancement and Layout Dependency Improvement by Using Atomic Layer Deposition SIN Spacer

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Abstract

By using Atomic Layer Deposition (ALD)-SIN spacer formation, the drive current of NMOS is improved due to the strain enhancement. Moreover, NMOS with ALD-SIN spacer shows small layout dependency such as gate pitch and Source Drain (SD) width. No reliability degradation is found from NBTI and HCI result.

Introduction

Not only enhanced transistor performance but also good control of various process fluctuations are strongly required.

MOS device with Dual Stress Liner (DSL) and SiGe-SD structure has been reported for promising strain control techniques for enhanced drive current [1,2,3]. Utilizing more effective local strain is important to improve transistor performance. The device with LPCVD-SIO spacer of compressive stress cannot enhance the drain current of NMOS. Spacer formation applied by tensile ALD-SIN is considered as key process to improve NMOS transistor performance.

Suppression of short channel effects (SCE) is also important for transistor performance. Thermal budget of ALD-SIN is lower than that of conventional LPCVD-SIO because of plasma assist. Therefore by utilizing ALD-SIN, suppressing SCE is also considered as superior characteristic not to occur extra impurities diffusion.

Spacer formation is an important factor to control the dependency of sparse and dense pitch. It is difficult to deposit film at dense pitch in the same way as sparse by using LPCVD-SIO. However ALD-SIN enables to deposit very thin SIN for every single layer. Therefore it is considered that ALD-SIN can improve gate pitch dependency.

Results and Discussion

We fabricated CMOS transistor in process flow, as shown in Fig. 1. For the key spacer formation, we used LPCVD-SIO, or ALD-SIN with lower thermal budget than LPCVD-SIO. Fig. 2 shows the sequence of ALD-SIN deposition. Fig2 . (a), (b) is NH_3 step. Fig.2 (c), (d) is SiH_2Cl_2 step. There is purge step between NH_3 step and SiH_2Cl_2 step. Fig. 3 shows the cross-sectional TEM image of 34 nm gate length NMOS with ALD-SIN spacer.

a. Transistor improvements

Fig. 4 compares the V_{th}-rolloff characteristics of ALD-SIN spacer with LPCVD-SIO spacer for NMOS. We can see there is no difference between the spacers. Fig. 5 shows I_{ds}-V_{ds} characteristics. At V_{ds}= 1 V and off current of 100 nA/μm, drain current (Ion) of 1150 μA/μm with gate length of 34 nm for NMOS was obtained. An 8% NMOS Ion improvement was achieved without change of PMOS drive current by applying ALD-SIN spacer, as shown in Fig. 6.

Fig. 7 shows the linear drive current (I_{dlin}) characteristic. I_{dlin} of ALD-SIN spacer device is 10% higher than that of LPCVD-SIO spacer device. I_{dlin} improvement appears superior mobility stressed by ALD-SIN spacer. Therefore it is found that NMOS channel stress was efficiently applied by using ALD-SIN spacer formation. Utilizing mobility and SCE improvement, superior I_{on}-I_{off} characteristic was achieved. Table 1 shows the value of major parameters among published data. Our device performance for NMOS is the highest I_{on} in the latest published data [4,5,6].

b. Layout dependency

Fig. 8 compares I_{on} of gate pitch dependency for ALD-SIN spacer with LPCVD-SIO spacer. The device with ALD-SIN spacer had smaller difference for sparse (gate pitch : 500nm) and dense (gate pitch : 200nm) than LPCVD-SIO spacer. ALD-SIN enables to deposit uniform thin film thickness independently of patterned indented substrate surface. Therefore the SEM measurement value of spacer width for sparse and dense pitch with ALD-SIN spacer width almost overlapped ideal line ,as shown in Fig. 9.

Fig. 10 also shows the dependency of I_{on} for SD width. It is found that I_{on} degradation of device with ALD-SIN spacer was smaller than LPCVD-SIO spacer for narrow SD width due to mobility improvement by local stress of ALD-SIN emphasized at narrow SD width.

c. Reliability

The concern of SIN spacer is HCI of I/O transistor and NBTI. Because ALD-SIN is Si-H bond free, they were not deteriorated, as shown in Fig. 11 and Fig. 12 [7,8].

Conclusion

We simultaneously presented to achieve high performance at 34 nm gate length and layout dependency improvement with ALD-SIN spacer for NMOS.

By applying ALD-SIN spacer, drive current of 1150 μA/μm were achieved at V_{ds} =1 V and off current of 100 nA/μm. This result is the highest I_{on} in the latest published data. Furthermore , the layout dependency such as gate pitch and SD width dependency were controlled very well.

References

[1] H.Ohta et al., *IEDM Tech. Dig.,pp.247-250, 2005* [2] H.Ohta et al., *Symp. on VLSI Tech. pp.222-223, 2006* [3] Y.S.Kim et al., *IEDM Tech. Dig.,pp.871-874, 2006* [4] H.Nii et al., *IEDM Tech. Dig.,pp.685-688, 2006* [5] M.Horstmann et al., *IEDM Tech. Dig.,pp.243-246, 2005* [6] Fu-Liang Yang et al., *Symp. on VLSI Tech. Dig.,pp.1070-1072, 2005* [7] K.Ichinose et al., *Symp. on VLSI Tech. Dig.,pp.103-104, 2001* [8] M.Yamamura et al., *VLSI Tech. Dig.,pp.88-89, 2005*

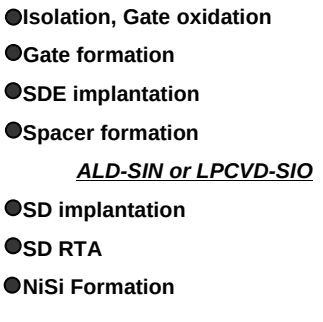

Fig. 1 CMOS process flow

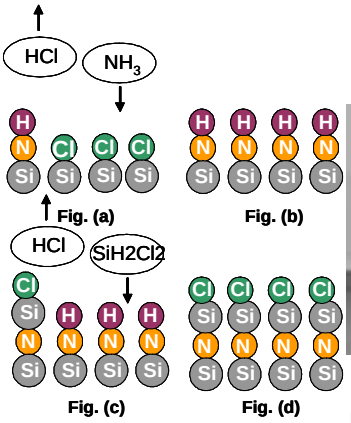

Fig. 2 ALD-SIN sequence

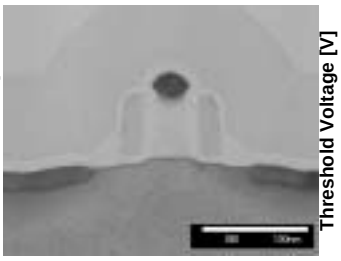

Fig. 3 TEM image of 34 nm NMOS with ALD-SIN spacer

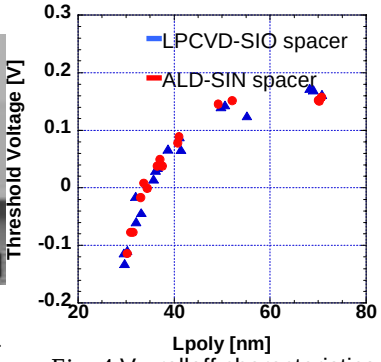

Fig. 4 V_{th}-rolloff characteristics of NMOS

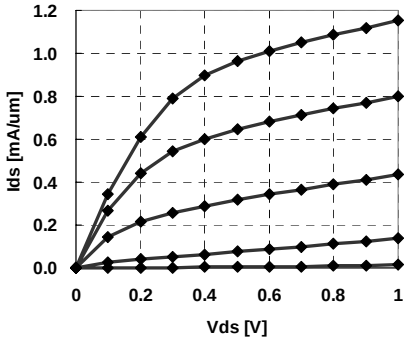

Fig. 5 I_{ds}-V_{ds} characteristics of 34 nm gate length NMOS

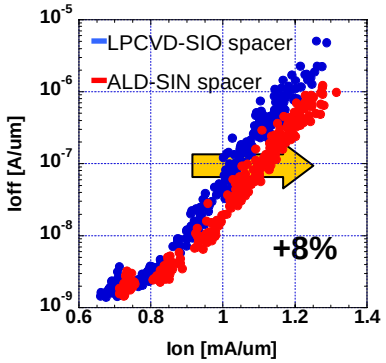

Fig. 6 I_{on} vs. I_{off} characteristics of at V_{dd}=1.0V

Table 1 Device performance comparison at V_{dd}=1.0V of NMOS

	This work	Ref.4	Ref.5	Ref.6
Lpoly [nm]	34	34	40	30
Vdd[V]	1	1	1	1
Ion[μA/μm]	1150	1100	1080	1000
Ioff[nA/μm]	100	100	200	100
Tinv[nm]	1.98	-	-	1.9
Ig[A/cm2]	28	30	-	-
Sub.	Bulk	Bulk	SOI	SOI

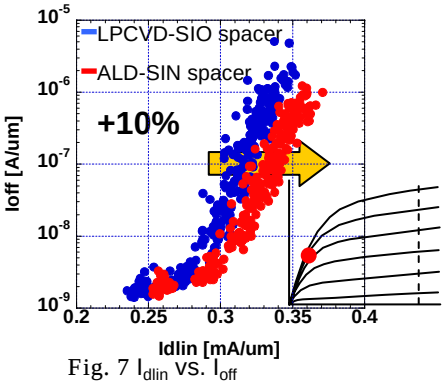

Fig. 7 I_{dlin} vs. I_{off} characteristics at V_{dd}=0.1V

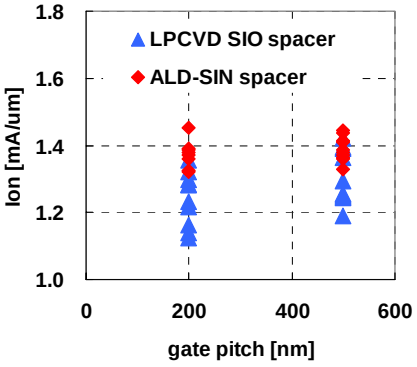

Fig. 8 I_{on} of gate pitch dependency of dense for NMOS

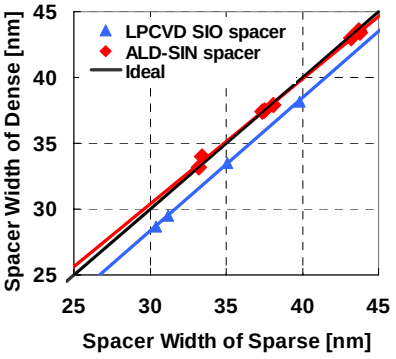

Fig. 9 SEM measurement value of width for sparse and dense pitch

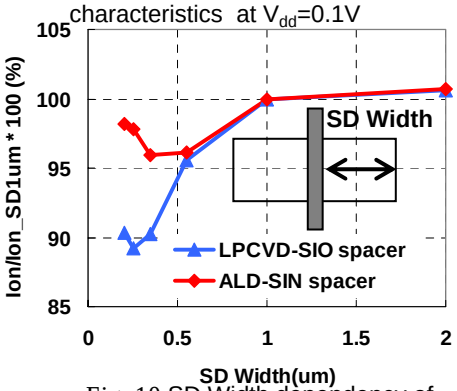

Fig. 10 SD Width dependency of 34 nm gate length for NMOS

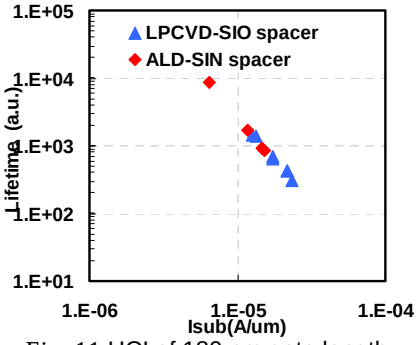

Fig. 11 HCI of 180 nm gate length of NMOS for ALD-SIN and LPCVD-SIO spacer (I/O Transistor)

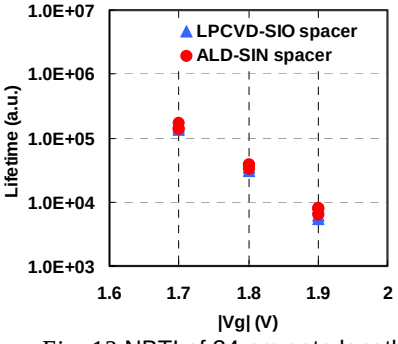

Fig. 12 NBTI of 34 nm gate length of PMOS for ALD-SIN and LPCVD-SIO spacer