Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 866-867

B-7-2

In-situ Doped Embedded-SiGe Source/Drain Technique for 32 nm-node pMOSFET

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Introduction

Compressive-channel-stressing process is indispensable for hole-mobility enhancement, and embedded-SiGe (e-SiGe) Source/Drain (S/D) technology is considered to be promising for realizing 32 nm-node pMOSFET [1-2]. When combining e-SiGe stressor with S/D extension (SDE) last process [3], two types of S/D deep junction formation are considered: one is the boron implantation after the formation of non-doped e-SiGe S/D regions (Fig. 1 (a)), and the other is the in-situ boron-doping during e-SiGe S/D process (Fig. 1 (b)). These processes have not been evaluated from a viewpoint of transistor performance. In this work, impacts of the S/D formation process on device performance are systematically investigated by analyzing channel stress and parasitic resistance. In addition, the optimized e-SiGe S/D technology applicable for 32 nm-node pMOSFET is demonstrated.

Comparison of Device Performance

Process sequences of pMOSFET with e-SiGe S/D stressor are illustrated in Fig. 1. The SDE last process, where SDE is formed after the deep junction process, is employed to realize shallow SDE. In this study, two device design schemes are studied: Device **A** in which boron is implanted to non-doped e-SiGe S/D and Device **B** in which S/D deep junction is formed by in-situ boron-doped e-SiGe. The SDE was formed after deep contact junction formation followed by nickel silicide process (Fig. 2). I_{ON}-I_{OFF} characteristics of pMOSFET (L_G = 35 nm) in Fig. 3, where off-current (I_{OFF}) is changed by channel implantation for each device, indicate that both e-SiGe S/D processes improve the device performance. It should be noted that the device with boron-doped e-SiGe (Device **B**) exhibits higher current-drive than that with non-doped e-SiGe (Device **A**). This performance difference is analyzed in the following section.

Analysis of Device Characteristics

Channel Stress

A smaller slope in R_{ON} vs. L_G indicates higher mobility in the channel region; therefore, the hole mobility of pMOSFET with the boron-doped e-SiGe process is higher than that with the non-doped e-SiGe process (Fig. 4). The channel stress of the non-doped e-SiGe process was measured by Nano Beam Diffraction (NBD) technique as shown in Fig. 5. Its compressive channel stress is 1.15 GPa after the non-doped e-SiGe growth: however, the channel stress reduces by about 40% after the S/D and SDE implantation. These results indicate that high dose and/or energy implantation leads to the significant relaxation of compressive channel stress, which degrades the hole mobility in the non-doped e-SiGe process. It is evident that the boron-doped e-SiGe S/D process is effective in preventing the relaxation of channel stress.

Tensile stress from cobalt silicide films has been reported [4]; accordingly, this is also the concern of pMOSFET performance degradation. The channel stress modulation from silicide formation was also evaluated by NBD technique where NiSi was utilized without SDE and deep junction implantation (Fig. 6). It is revealed that the relaxation of compressive stress is negligible due to less silicon consumption in NiSi films than in $CoSi_2$ films.

Parasitic Resistance

Components of parasitic resistance such as silicide/silicon contact resistance (R_C), sheet resistance of deep junction beneath silicide films (R_D) and silicide sheet resistance (R_{SH}) were extracted from the fabricated devices. The decrease of R_C in the e-SiGe S/D is mainly due to Schottky barrier height lowering by Ge incorporation (Fig. 7 (a)). Highly activated, box-shaped S/D of the boron-doped e-SiGe markedly reduces R_D. (Fig. 7 (b)). R_{PARA} originating in the silicide films (R_{CO}) at the source or drain was calculated on the basis of the transmission line model for silicided diffusions [5] (Fig. 7 (c)). The boron-doped e-SiGe process substantially reduces R_C and R_D, thus providing the lowest R_{PARA}.

Scalability of e-SiGe S/D for 32 nm-node Technology

Placement of the boron-doped e-SiGe close to the channel region increases the hole mobility; however, it degrades V_{TH} roll-off because of boron diffusion from the doped SiGe [6]. To overcome this trade-off, recessed Si-shape and the distance from the gate to the e-SiGe S/D ($L_{G\text{-}SiGe}$) are optimized (Fig. 8). Optimization of the recessed Si-shape suppresses the boron diffusion (1 ➔ 2 in Fig. 9), which reduces the short-channel effect. Moreover, scaling $L_{G\text{-}SiGe}$ enhances the current-drive without degrading short channel effect immunity (2 ➔ 3 in Fig. 9). Therefore, it is demonstrated that precise control of the recessed Si-shape and e-SiGe proximity drastically improves device performance, satisfying 32 nm-node requirements.

Layout dependence of device performance is also important [7-8]. Scaling S/D diffusion length (L_{SD}) considerably degrades the current drive (Fig. 10). As compared to L_{SD} = 1000 nm, the performance degradation at L_{SD} = 250 nm is approximately 10% at L_G = 35 nm. Meanwhile, in the case of one generation advance from 45 nm-node to 32 nm-node, L_{SD} scaling results in only 1.0% degradation in current drive because of the high-volume (thick) and properly designed e-SiGe structure. On the other hand, performance improvement by L_G scaling from 45 nm-node to 32 nm-node becomes 5.0% (Fig. 11). Consequently, the improvement by L_G scaling overcomes the degradation of transistor performance by L_{SD} scaling. These results confirm that the boron-doped e-SiGe S/D stressor technology is one of the promising technique for realizing 32 nm-node pMOSFET.

Conclusion

The boron-doped e-SiGe S/D structure significantly enhances hole mobility and reduces R_{PARA} for 32 nm-node pMOSFET. Precise control of the recessed Si-shape and continual gate length scaling is the key for the boron-doped e-SiGe stressor process.

References

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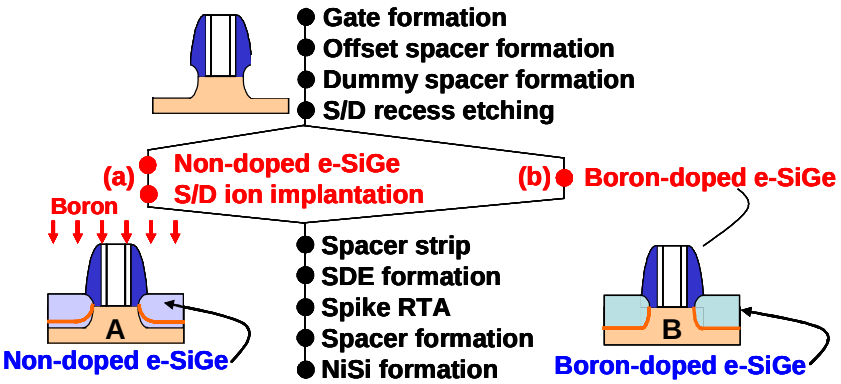


Fig.1 Process sequences of pMOSFET with e-SiGe S/D process.

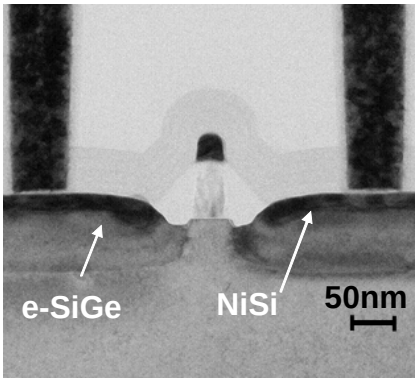


Fig.2 Cross-sectional TEM image of Device **A** pMOSFET (L_G = 35 nm).

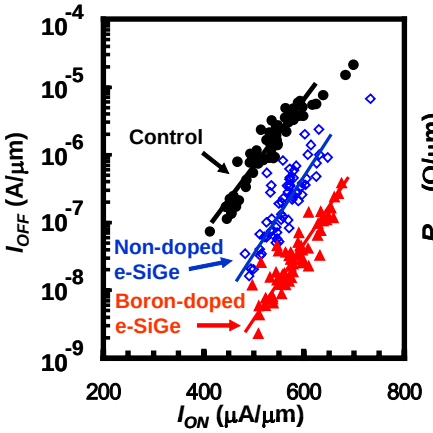


Fig.3 I_{ON}-I_{OFF} characteristics (L_G = 35 nm). I_{OFF} is changed by channel implantation.

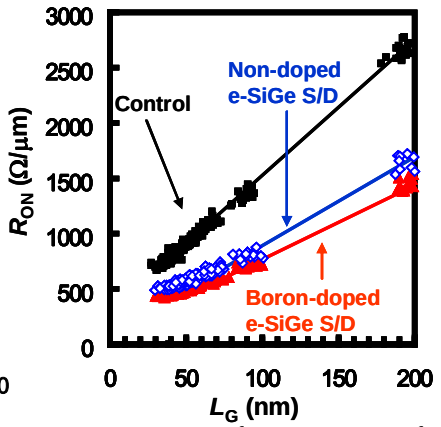


Fig.4 R_{ON} vs. L_G for various types of transistor structures. Smaller slope indicates the higher hole-mobility.

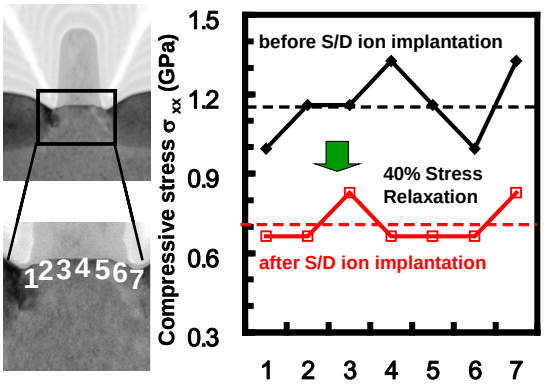


Fig.5 Channel stress at 7 spots in the channel. From NBD measurement, 40% relaxation of compressive stress due to ion implantation is observed.

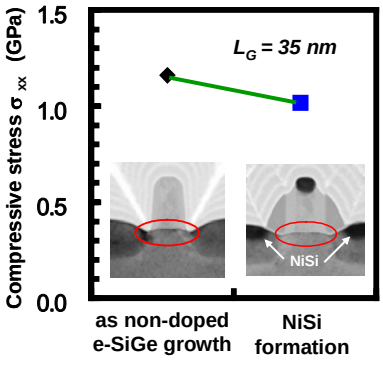


Fig.6 Impact of the tensile stress from NiSi on the channel stress.

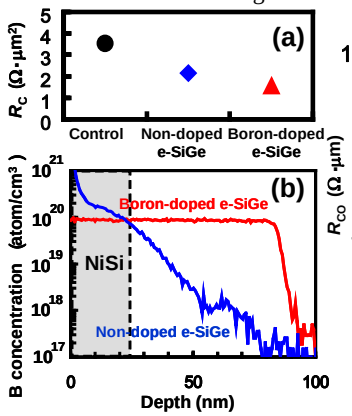
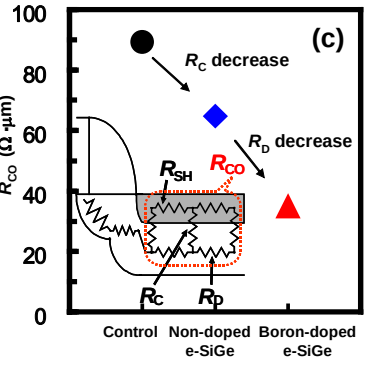


Fig.7 (a) Silicide/silicon R_C, (b) SIMS depth profile of boron, (c) R_{CO} decrease by the reduction of silicide/Si R_C and R_D. Boron-doped e-SiGe process is advantageous for smaller R_{PARA}.



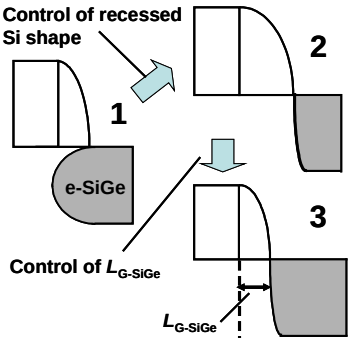


Fig.8 Optimization of boron-doped SiGe S/D structure. Precise control of recessed-Si shape and $L_{G\text{-}SiGe}$ is needed.

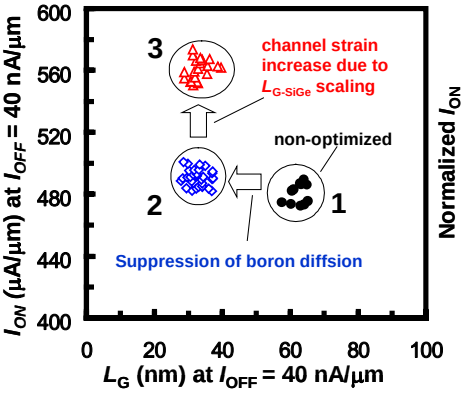


Fig.9 L_G-I_{ON} characteristics for various device structures shown in Fig. 8.

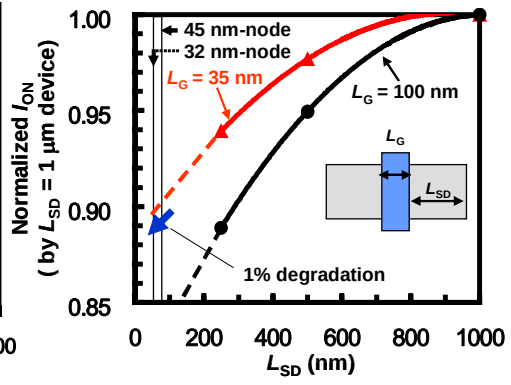


Fig.10 Current-drive degradation by the scaling of S/D diffusion lengths (L_{SD}).

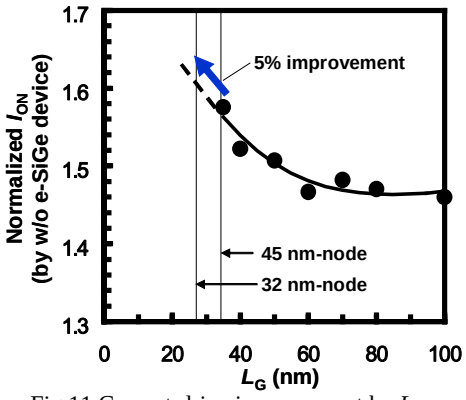


Fig.11 Current-drive improvement by L_G scaling. This improvement overcomes the degradation by L_{SD} scaling.