B-7-3

Principal Guideline of Stress Design for Ion Enhancement in Advanced MOSFET Structure with Dual Stress Liner Technique

M. Nishikawa, H. Nomura, T. Miyashita*, M. Kojima, Y. Takao and K. Hashimoto

Fujitsu Limited, *Fujitsu Laboratories Limited, 50 Fuchigami, Akiruno, Tokyo 197-0833, Japan
Phone: +81-42-532-1254, Fax: +81-42-532-2513, Email: m_nishikawa@jp.fujitsu.com

Abstract

This paper describes factors affecting a layout boundary dependence of mobility caused by dual stress liner (DSL). We have demonstrated how it can affect the device performance by simulations in good agreement with experiments. It is found that these variations of dependence are attributed to "inflection point" of contact etch stop layer (CESL). Moreover, it is clarified that thinner CESL thickness and shrinkage of sidewall spacer are significant to suppress CESL boundary dependence due to the proximity of inflection point. These findings give us appropriate guideline to design the structure of sidewall spacer as the optimization of stress transfer.

I. Introduction

In recent years, process-induced strain technology, such as CESL is widely used for improvement of electrical performances in scaled device [1, 2]. It has been well developed for the transistor architecture, that is, tensile CESL (tCESL) for NMOS, and compressive CESL (cCESL) for PMOS [3, 4]. In order to adopt the strain engineering as a key component of the device architecture, detailed understanding of process-induced stress distribution and its modeling have become important for scaled CMOS devices. There are many investigations of CESL stress dependence on the layout parameters, such as stacked layout, contact hole pitch, and poly-to-contact distance [5-8]. These parameters affect layout boundary dependence and mobility enhancement. However, there are few reports including the mechanism of CESL layout dependence affected by other layout parameters, such as CESL thickness and sidewall spacer width. In this paper, we explore in-depth the origin of these factors impact on layout boundary dependences. We also present the guideline for suppression of boundary dependence.

II. Methodology

A simplified 45 nm device structure shown in Fig. 1 is studied in this paper. 2D stress distributions are simulated by commercially available TCAD tools [9]. We used the relationship between mobility improvement and stress, which is well described by linear piezoresistivity effect [10]. In the relationships, mobility along transport x direction is determined by stress along both the transport and width directions, as

$$\mu xx = \mu_0 \left(1 - \Pi_{//} Sxx - \Pi_{12} Syy - \Pi_{\perp} Szz \right), \qquad (1)$$

where μ_0 denotes the isotropic mobility without stress, μ_{ij} is the mobility under stress **S** in the six-component vector, and Π_{ij} are piezoresistive coefficients for carriers. The piezoresistive coefficient for bulk silicon is reported in [11]. The x-axis is aligned to the <110> crystal axes (channel direction) in the (100) plane. Table I summarizes experimental piezoresistive coefficients which are we used in (1), and the calculated components from TCAD tools are also imported into (1).

III. Result and Discussion

Fig. 2 shows simulated SLx dependence of stress (a) Sxx and (b) Syy. SDW is source and drain width. SLx is the distance from active edge to CESL. Outside the boundary is neutral CESL (without DSL integration) or inverse polarity (with DSL integration), cCESL and tCESL for NMOS and PMOS, respectively. The reasonable tendencies are obtained, that is, proximity of boundary degrades the benefit of CESL because of inverse polarity. In Sxx and Syy on NMOS, DSL integration introduces twice as large SLx dependence as that without DSL since cCESL has higher intrinsic stress than that of tCESL. In Fig. 3, we show that simulated stress distributions of (a) NMOS and (b) PMOS. It is observed that there are some regions where stress is highly concentrated due to the inflection formed by the shape of sidewall spacer (corresponding to encircled parts). The Stress by CESL is observed for transferring to the channel by way of sidewall spacer from this point. Hence, inflection point is believed to play critical roll in transfer of CESL stress structurally. Fig. 4 shows measurements of linear current, Idlin (Vd = 0.02 V, Vg = 1.0 V), SLx dependence (a) NMOS and (b) PMOS compared to simulated results. It is confirmed that the simulated results are consistent with all

qualitative behaviors on the measurements.

In order to investigate the impact of inflection point, we show measured Idsat dependences on SLx for various CESL thicknesses (from 70 to 100 nm), together with the simulated results in Fig. 5 (a) NMOS and (b) PMOS. All simulated results are in good agreement with experiments qualitatively. The sensitivity for SLx is observed to be lager with increasing thickness. In Figs. 6 and 7, we show simulated distributions of Sxx for NMOS and PMOS, respectively. CESL thickness is (a) 70 nm and (b) 100 nm. It can be observed that the distance from channel edge to inflection point is smaller for the case of thinner thickness. In other words, if inflection point is away from the channel edge, the layout dependency is more sensitive to SLx. Thus, the stress at inflection point is more dominant than that of CESL boundary.

Next, we compared Sxx of the two kinds of transistors with and without sidewall spacer by the simulation in order to confirm the effect of inflection point as shown in Fig. 8. As a result, the transistor without sidewall spacer shows 28 % and 17 % larger stress than that with sidewall spacer for NMOS and PMOS, respectively. It is noted that changing sidewall spacer width affects the boundary dependence strongly related to inflection point. Such narrower sidewall spacer has been previously reported in terms of stress transfer as a key technology for current enhancement in [12]. In addition, we show simulated stress distributions of transistor without sidewall spacer in Fig. 9 (a) NMOS and (b) PMOS. It is observed that the stress from inflection point is more effectively transferred to the channel because of sidewall spacer-less structure. Fig. 10 shows comparison of SLx dependences on these transistors by simulation. SLx dependence is observed to be clearly smaller on the transistor without sidewall spacer due to the proximity of the inflection point. These results are the evidence regarding the relationship between inflection point and the trend of dependence. Note that the shrinkage of sidewall spacer is effective not only to suppress CESL boundary dependence, but also to improve device performance in terms of stress transfer. Furthermore, narrower sidewall spacer is appropriate for the trend of device scaling. Finally, it is demonstrated that the suppression of CESL boundary dependence is critically derived from the proximity of inflection point as shown in Figs. 5 and 10.

IV. Conclusions

The layout parameters impact on CESL boundary dependence were explored. We have demonstrated that "inflection point" is the origin of the variation on layout dependences by simulations which are in good agreement with experiments. Consequently, it is clarified that thinner CESL thickness and narrower sidewall spacer width are effective for the suppression of CESL boundary dependence. These findings can be the guideline to design the structure of sidewall spacer for the optimization of stress transfer, and significantly improve understanding the layout dependence.

References

[1] K. Goto et al., IEDM Tech. Dig, pp. 209, 2004. [2] P. Grudowski et al., Symp. VLSI Tech. Dig., pp. 62, 2006. [3] S. Pidin et al., IEDM Tech. Dig, pp. 213, 2004. [4] H. Yang et al., IEDM Tech. Dig, pp. 1075, 2004. [5] T. Miyashita et al., Ext. Abst. SSDM, pp. 170, 2006. [6] R. Liebmann et al., SISPAD, pp. 173, 2006. [7] S. Cea, et al., IEDM Tech. Dig, pp. 963, 2004. [8] F. Payet et al., Ext. Abst. SSDM, pp. 176, 2006. [9] TSUPREM-4 reference manual. [10] X. Wang et al., SISPAD, pp. 323, 2005. [11] K. Matsuda et al., J. Appl. Phys., **73**(4), pp. 1838, 1993. [12] Y Liu et al., IEDM Tech. Dig, pp. 836, 2005.

Table I. Piezoresistance coefficients for Si (001) surface in units of 10^{-12} cm^{2}dyn^{-1}[10].

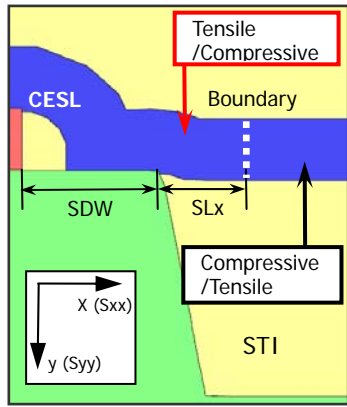| Stress		<110>	<001>	<1-10>
		$\Pi_{//}$	Π_{12}	$\Pi_{\perp}$
PR coeff.	NMOS	-22	33	-10
	PMOS	48	3	-49

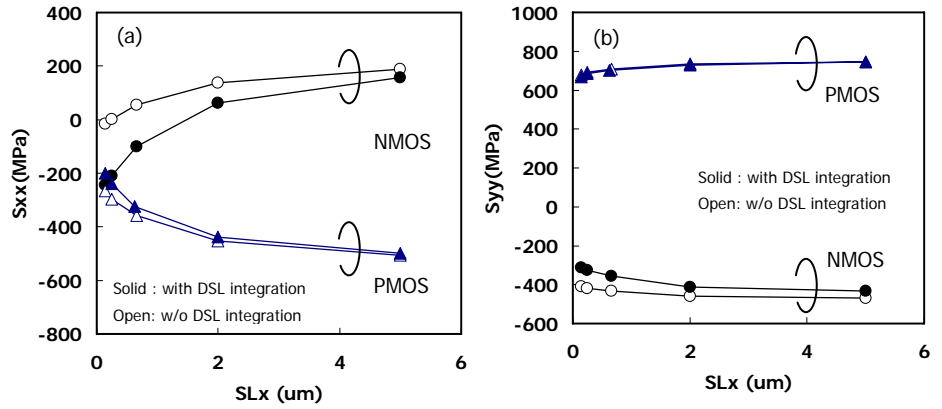Fig. 1 Example of 2D structure of half device with CESL and its boundary.

Fig. 2 Simulated SLx dependence of stress. Stresses were averaged along <110> channel at the depth of 1nm below the oxide interface. The layout is SDW = 1.0 um and W = ∞. (a) Sxx and (b) Syy.
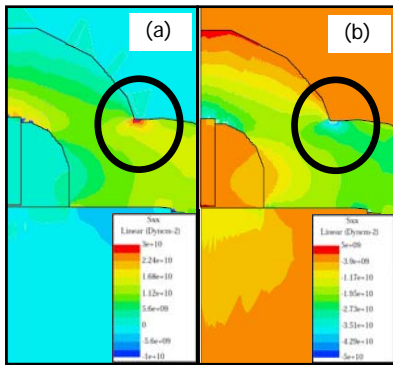

Fig. 3 Simulated Sxx distribution of 2D structure in Fig. 1. An encircled region shows "inflection point". (a) NMOS and (b) PMOS.
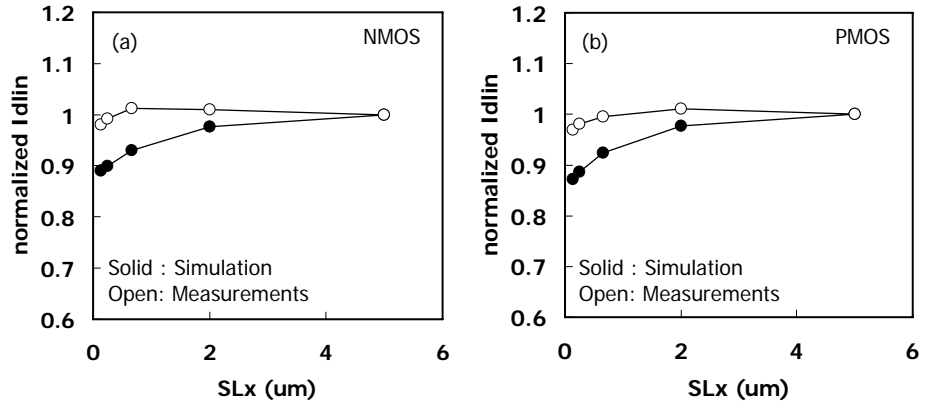

Fig. 4 Measured normalized Idlin vs. SLx compared to simulations with piezoresistance coefficients on Table I. Data were normalized at SLx = 5 um. The layout is SDW =1.0 and W = 10 um on measurement data with DSL integration. (a) NMOS and (b) PMOS.
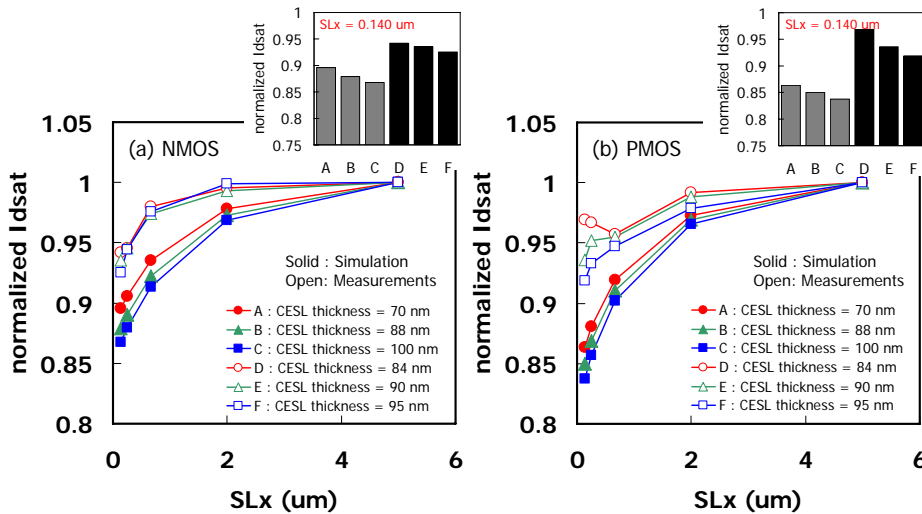
Fig. 5 Measured normalized Idsat vs. SLx compared to simulations with variation of CESL thickness. Data were normalized at SLx = 5 um. CESL thickness is varied from 70 to 100 nm. Inset shows normalized Idsat for each devices, extracted at SLx = 0.14 um. (a) NMOS and (b) PMOS.
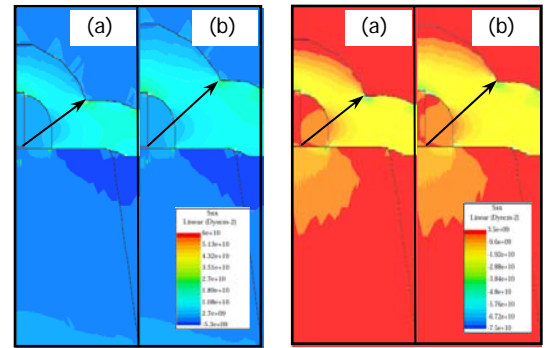

Fig. 6 Simulated Sxx distributions of NMOS with DSL integration. (a) CESL thickness is 70 nm and (b) CESL thickness is 100 nm. The arrows show the distance from channel edge to inflection point.
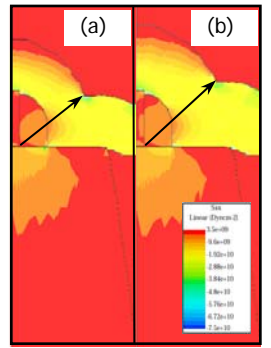

Fig. 7 Simulated Sxx distributions of PMOS with DSL integration. (a) CESL thickness is 70 nm and (b) CESL thickness is 100 nm. The arrows show the distance from channel edge to inflection point.
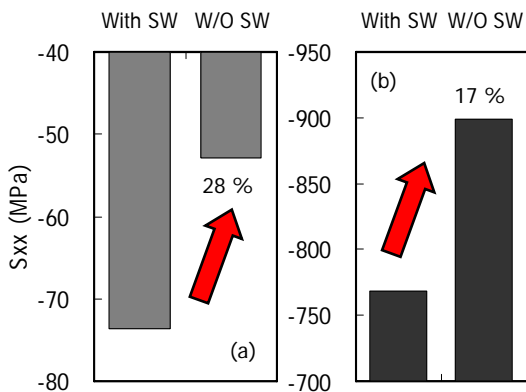

Fig. 8 Simulated Sxx on the devices with and without sidewall spacer. (a) NMOS and (b) PMOS.
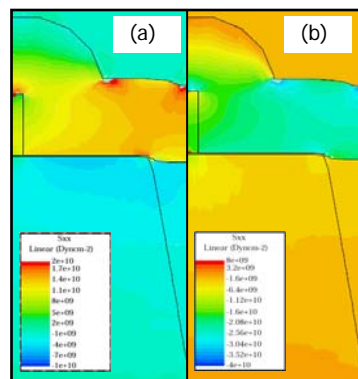

Fig. 9 Simulated Sxx distribution of the transistor without sidewall spacer. (a) NMOS and (b) PMOS.
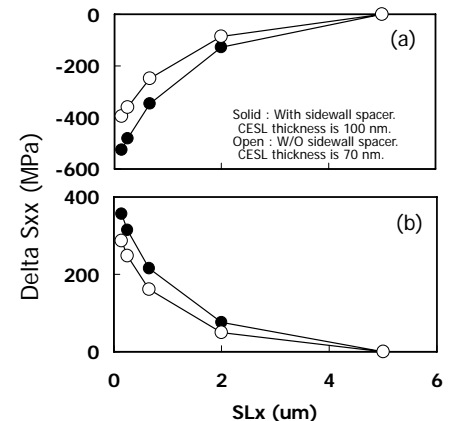

Fig. 10 Simulated SLx dependence of Sxx. Sxx at each SLx is subtracted Sxx at SLx = 5um as delta Sxx. (a) NMOS and (b) PMOS.