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Study of Stress from Discontinuous SiN Liner for Fully-Silicided Gate Process

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1. Introduction

Enhancement of carrier mobility using a strained-Si technology and elimination of gate-depletion using a metal gate are significant for performance improvements of miniaturized MOSFETs. Induction of channel strain utilizing a high-stress SiN film as a contact etch stopper layer (CESL) has been reported as one of the strained-Si technologies [1-4]. As a metal gate, fully-silicided (FUSI) gate has been studied as a candidate for next generation CMOS [5-7], because it has a high consistency with the conventional MOSFET process with a poly-Si gate. In FUSI gate process, it's usually necessary to planarize interlayer insulators and expose poly-Si gate top-surfaces before silicidation. At the same time, SiN-CESL of gate top-surface is also removed. It is considered that such discontinuous CESL induces different channel strain as compared with the conventional continuous CESL.

In this paper, effects of disconnection of high-stress SiN-CESL on a gate-top are investigated with a focus on FUSI gate process. Characteristics of poly-Si gate MOSFETs with discontinuous CESL are compared with that with continuous CESL for several SiN-stress conditions. Characteristics of Ni-FUSI gate MOSFETs with high-stress SiN-CESL are also discussed. It is demonstrated that discontinuous CESL still works, and the mobility enhancement utilizing a high-stress SiN film is also effective for FUSI process.

2. Experimental

Fig. 1 schematically shows the process flow. A 2-nm-thick plasma-nitrided oxide was used for a gate dielectric. After poly-Si deposition, gate doping was performed for NMOS and PMOS. Then hard-mask SiN was deposited and gate pattering was implemented. S/D-extension implantation, halo implantation, sidewall formation, deep-S/D implantation, and activation spike-RTA were implemented using the conventional techniques. Then 5-conditions of SiN-CESL were deposited: 60nm-thick and 30nm-thick SiN films with 1.7GPa tensile stress, a 20nm-thick SiN film with 1.3GPa tensile stress (control), and 30nm-thick and 60nm-thick SiN films with 2.4GPa compressive stress. After inter-layer SiO_2 deposition and CMP planarization, samples were split into 3 structures: a control poly-Si gate sample with continuous CESL, a poly-Si gate sample with discontinuous CESL, and a Ni-FUSI gate sample with discontinuous CESL. Fig. 2 shows the cross-sectional SEM images of samples with discontinuous CESL. It can be seen that the gate-top SiN-CESL was successfully removed for both the poly-Si gate and the FUSI gate samples.

3. Results and Discussion

At first, comparisons are made for the poly-Si gate samples with continuous CESL and those with discontinuous CESL. Fig. 3(a) shows nMOSFET I_{on}-I_{off} characteristics of the poly-Si gate with continuous CESL and their dependence on the SiN stress, and Fig. 3(b) shows those for the poly-Si gate with discontinuous CESL. The drive current of the discontinuous CESL increases with the increase in the tensile stress as well as that of the continuous CESL. As for pMOSFET in Fig. 4, the drive current increases with the increase in the compressive stress for both the continuous and discontinuous CESL. It is found that drive current is modified by stress and thickness of SiN-CESL, even if CESL is disconnected on the gate-top.

Fig. 5 shows the dependence of $G_{m,max}$ on the CESL stress. In Fig. 5, the horizontal-axis represents the product of SiN stress and its deposited thickness, and the vertical-axis represents $G_{m,max}$ normalized by that of the sample with a 20nm-thick SiN film with 1.3GPa tensile stress. The dependence of $G_{m,max}$ on SiN-stress is more significant for Lg=100nm than for Lg=1μm, which is the feature of mobility modulation by CESL [3]. Fig. 5 also includes the FUSI gate sample. It can be seen that the dependences of $G_{m,max}$ on SiN-stress have same tendency but different slopes for 3 structures.

Stress simulation was implemented to verify the effect of CESL discontinuity. Fig. 6 schematically shows the simulated structure. The height and length of gate poly-Si was 120nm and 100nm, respectively. Initial thickness of SiN-CESL was 60nm, and its removed thickness from gate-top was a parameter. Fig. 7 shows the dependence of channel (Si-surface) stress on the removed thickness. For both tensile and compressive SiN, the stress of X-direction is increases and that of Z-direction is decreases with the increase in the removed thickness of SiN-CESL. In the case of nMOSFET and tensile CESL, for an example, increase of X-stress increases I_{ds} and decrease of Z-stress decreases I_{ds}. They are considered to be balancing the effect of disconnection of CESL on the mobility. As a result, the continuous CESL and the discontinuous CESL have dependence on the stress of CESL in qualitatively the same but quantitatively the different manner. In addition, for FUSI gate, the stress from gate-electrode should be considered, which was not included in this simulation.

4. Conclusions

Effects of high-stress SiN-CESL on fully-silicided gate process are investigated. Characteristics of poly-Si gate MOSFETs and Ni-FUSI gate MOSFETs with discontinuous CESL are compared with that of poly-Si gate MOSFETs with continuous CESL for several SiN-stress conditions. It is demonstrated that the discontinuous CESL works as well as the continuous CESL, although their simulated distributions of channel stress are not same. Mobility enhancement utilizing a high-stress SiN film is applicable for FUSI gate process.

References

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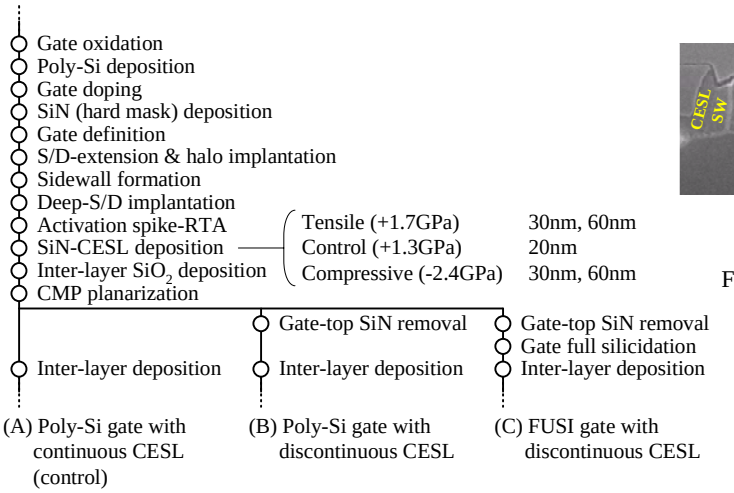
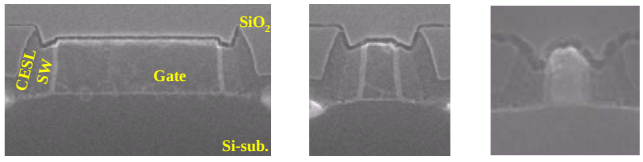
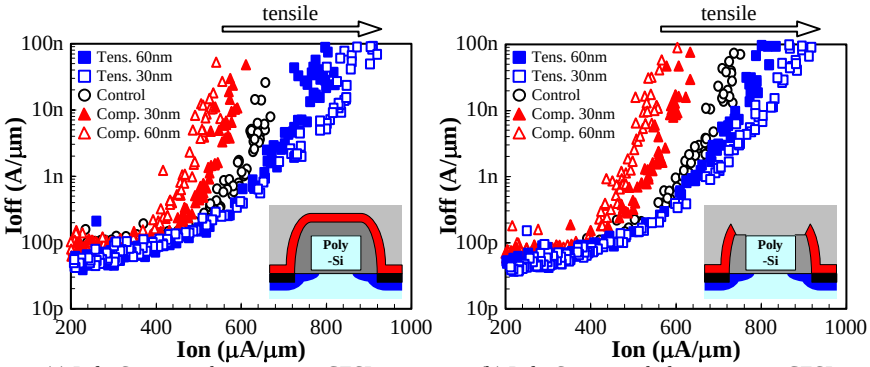


Fig. 1. Schematic process flow.



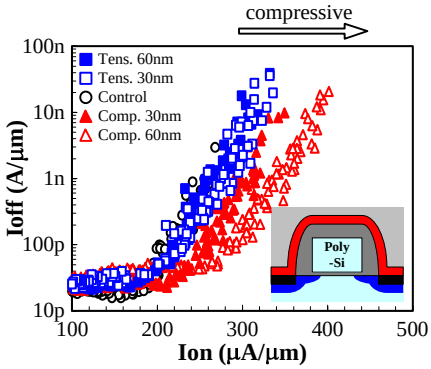
(a) Poly-Si gate, Lg~360nm (b) Poly-Si gate, Lg~70nm (c) Ni-FUSI gate, Lg~65nm

Fig. 2. Cross-sectional SEM image of discontinuous CESL.

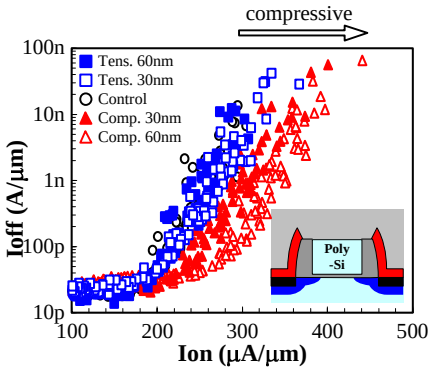


(a) Poly-Si gate with continuous CESL (b) Poly-Si gate with discontinuous CESL

Fig. 3. Dependence of Ion-Ioff characteristics of poly-Si gate NMOSFET on SiN-CESL.



(a) Poly-Si gate with continuous CESL



(b) Poly-Si gate with discontinuous CESL

Fig. 4. Dependence of Ion-Ioff characteristics of poly-Si gate PMOSFET on SiN-CESL.

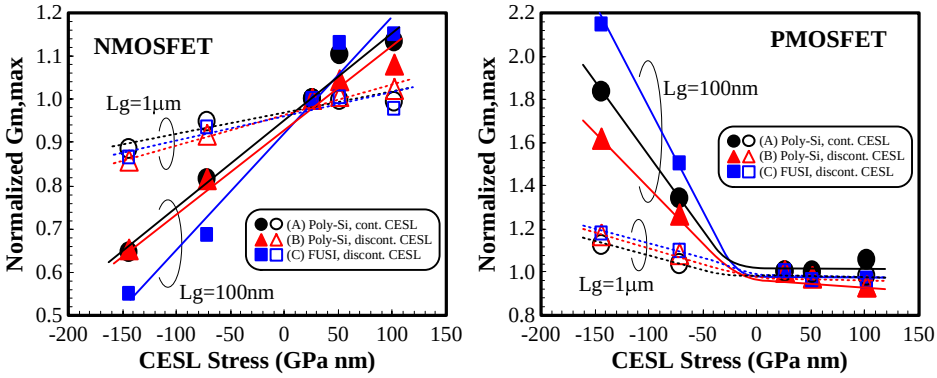


Fig. 5. Comparison of Gm,max as a function of CESL stress for 3 structures. X-axis is product of SiN stress and its thickness. Y-axis is normalized at 1.3-GPa and 20-nm SiN.

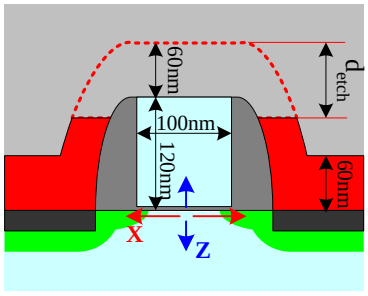
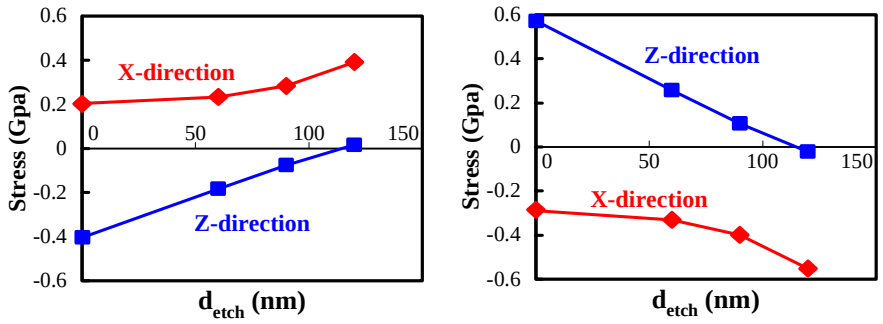


Fig. 6. Schematic cross-sectional view of stress simulation. Thickness of deposited SiN-CESL is 60nm and thickness of removed SiN-CESL is expressed as d_{etch}.



(a) Tensile CESL (+1.7GPa) (b) Compressive CESL (-2.4GPa)

Fig. 7. Dependence of simulated channel stress on thickness of removed SiN-CESL.