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Strained N-channel FinFETs with High-stress Nickel Silicide-Carbon Contacts and Integration with FUSI Metal Gate Technology

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1. Introduction

Several reports have shown the effectiveness of strained-silicon technology for enhancing performance in multiple-gate transistors [1]-[4]. In particular, silicon-carbon (SiC) source and drain (S/D) stressors have been demonstrated to yield significant I_{Dsat} enhancement in both n-channel planar and multiple-gate transistors [5]. In this work, we demonstrate the first successful integration of FinFETs incorporating SiC S/D regions with nickel silicide-carbon (NiSi:C) contacts. (Note: We denote silicided S/D regions where contacts will be eventually formed as "contacts" for brevity throughout this abstract.) We further show that stress in the NiSi:C film can be tuned and exploited to induce significant amounts of additional tensile channel strain for performance enhancement. Lastly, we report the successful integration of FinFETs with NiSi:C stressors with fully-silicided (FUSI) metal gate technology, which dramatically improves I_{Dsat} performance as a result of improved electrostatic control and additional gate-induced channel strain.

2. Tuning stress levels in NiSi and NiSi:C silicides

The evolution of sheet resistance and film stress in NiSi and NiSi:C films with additional post-silicidation annealing was investigated. Two-step Ni silicidation was carried out on two wafers in a single wafer rapid thermal furnace (SRTF), using ~30 nm of deposited Ni. The first and second anneal steps were performed in N_2 ambient at 320˚C for 10 min and 400˚C for 10 min respectively. Prior to silicidation, 40 nm of $Si_{0.99}C_{0.01}$ was epitaxially grown on one wafer. Formation of the NiSi:C layer fully consumes the $Si_{0.99}C_{0.01}$ film.

After two-step silicide formation, these wafers were subjected to cumulative isochronal annealing (10 min) in a SRTF at temperatures ranging from 400˚C to 800˚C. After each anneal, sheet resistance and wafer curvature measurements were performed to monitor the evolution of sheet resistance and film stress in the NiSi and NiSi:C films (Fig. 1). It is observed that the sheet resistance of NiSi remains relatively constant from a temperature range of 400˚C to 650˚C. Above 650˚C, the sheet resistance of NiSi progressively degrades due to a combination of $NiSi_2$ phase transformation and agglomeration. For NiSi:C, the sheet resistance gradually improves with annealing at higher temperatures. SEM analysis of the film surfaces shows good surface morphology for the NiSi:C even after annealing at 800˚C, confirming its excellent thermal stability. These results concur with that reported in Ref. [6].

From Fig. 1, it can be seen that stress in a NiSi:C film increases from its initial value of ~0.6 GPa to ~1.0 GPa, after annealing at temperatures greater than 550˚C. As such, the high stress properties of NiSi:C films can be exploited when they are used to form contacts in n-channel devices, giving rise to increased longitudinal tensile channel stress.

3. Strained FinFETs with silicide-induced strain

The integration of NiSi:C contacts with double-gate FinFETs incorporating raised SiC S/D regions is explored. The FinFET fabrication flow is basically similar to that previously reported in Ref. [4]. Fig. 3 shows key steps in the process flow. Three experiment splits were fabricated, in which one was fabricated with low stress (LS) NiSi:C contacts. On two other splits, high stress (HS) NiSi:C contacts were employed. On one of these two splits, the gate hardmask was removed prior to silicidation, allowing the formation of a high-stress FUSI metal gate. The differences in the splits are summarized in a schematic (Fig. 4). Fig. 5(a) shows a tilted-SEM image of a FinFET device with HS NiSi:C S/D and poly-Si gate, while Fig. 5(b) shows a tilted-SEM image of a FinFET device with HS NiSi:C S/D and FUSI metal gate. The corresponding TEM image of such a device is shown in Fig. 5(c). Energy dispersive spectrometry (EDS) was used to aid in material analysis.

Fig. 6 shows the I_{Off}-I_{On} figure-of-merit. At an I_{Off} of 1 x 10^{-7} A/μm, FinFETs with HS NiSi:C contacts show ~14 % I_{On} improvement over control FinFETs with LS NiSi:C contacts. Significant I_{On} enhancement of ~40 % over control was obtained in FinFETs with both HS NiSi:C contacts and FUSI metal gate. The distributions of subthreshold swing (*SS*) and peak G_m of the same sets of devices are plotted in Fig. 7. It can be seen that FinFETs with LS and HS NiSi:C contacts have comparable *SS*. FinFETs with HS NiSi:C contacts and FUSI metal gate have improved *SS* due the absence of poly-depletion. Using HS NiSi:C contacts improves the peak G_m, suggesting strain-induced mobility enhancement. Integration of such devices with FUSI metal gate further enhances the peak G_m. This is attributed to increase in C_{ox} as well as FUSI gate stress effects.

A pair of FinFETs with LS and HS NiSi:C contacts were selected for comparison. Fig. 8 plots the I_{DS}-V_{GS} and G_m-V_{GS} characteristics, showing comparable subthreshold characteristics (comparable gate lengths and fin widths), as well as a 24 % enhancement in peak G_m. S/D series resistances were extracted from the asymptotic curves of total resistance R_{tot} plotted against gate overdrive V_{GS}-$V_{t,lin}$ (Fig. 9). The estimated S/D series resistances were found to be comparable. At a gate-overdrive of 1.2 V, I_{Dsat} was enhanced by 14 % due to higher longitudinal tensile channel stress induced by the HS NiSi:C contacts (Fig. 10). Fig. 11 compares the same device with HS NiSi:C contacts to another device with HS NiSi:C contacts and FUSI metal gate. Similarly, the subthreshold characteristics of this pair of devices are comparable. Peak G_m is significantly enhanced by 64 %. This large G_m enhancement has to be partially attributed to gate stress-induced electron mobility enhancement, since the increase in C_{ox} due to metal gate alone cannot account for the large enhancement. FUSI gate-induced channel stress effects have been summarized in Ref. [7]. Furthermore, no degradation in gate leakage current was found. Gate stress effects, together with increase in C_{ox}, give rise to a further 32 % enhancement in I_{Dsat} (Fig. 12). This translates to a 50 % I_{Dsat} enhancement over the control device with LS NiSi:C contacts, by employing both HS NiSi:C contacts and FUSI metal gate.

4. Conclusions

NiSi:C is a thermally stable contact material for SiC S/D devices. Tensile stress in NiSi:C can be increased using post-silicidation anneals. In FinFETs with SiC S/D regions, HS NiSi:C contacts give an additional 14 % I_{Dsat} enhancement over FinFETs with LS NiSi:C contacts. These results show that HS NiSi:C contacts can potentially have a synergistic effect when used in conjunction with embedded SiC S/D stressors. Successful integration of devices with HS NiSi:C contacts and FUSI metal gate proves its compatibility. At a given I_{Off} of 1 x 10^{-7} A/μm, the combination of these two techniques can provide up to 50 % I_{Dsat} enhancement.

References

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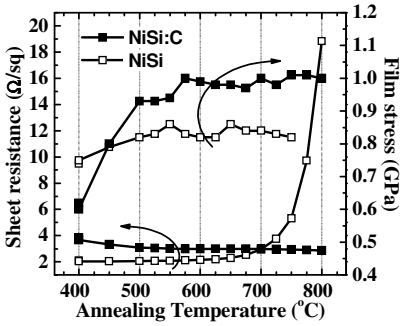

Fig. 1. Evolution of silicide sheet resistance and film stress with post-silicidation annealing.

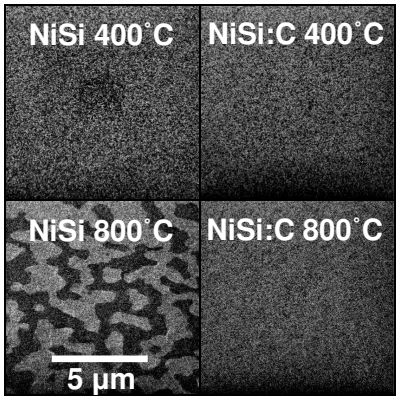

Fig. 2. SEM images showing good thermal stability of NiSi:C compared to NiSi.

- Channel implant
- Fin definition
- SiO_2 gate oxidation (18 Å)
- Poly-Si gate deposition and Gate implant
- Gate definition
- SDE implant
- Spacer formation (35nm) with stringer removal
- **Selective Epitaxial Growth of $Si_{0.99}C_{0.01}$**
- S/D implant and RTA activation
- **Gate hardmask removal for: "HS NiSi:C + FUSI Gate" split**
- Two-step Ni silicidation (20 nm Ni deposition, RTA 320˚C, excess Ni wet etch, and RTA 400˚C)
- **Stress-enhancing RTA anneal (600˚C) for: "HS NiSi:C" and "HS NiSi:C + FUSI Gate"**
- PECVD ILD (SiO_2) deposition and metallization

Fig. 3. FinFET fabrication process flow. A post-silicidation anneal enhances silicide stress.

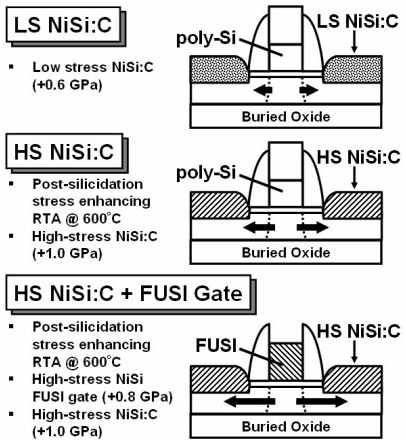

Fig. 4. Schematic showing the 3 experiment splits. In "HS NiSi:C" and "HS NiSi:C + FUSI Gate" splits, a post-silicidation stress enhancing anneal was performed. In the "HS NiSi:C + FUSI Gate" split, longitudinal tensile channel stress increases due to gate stress effects.

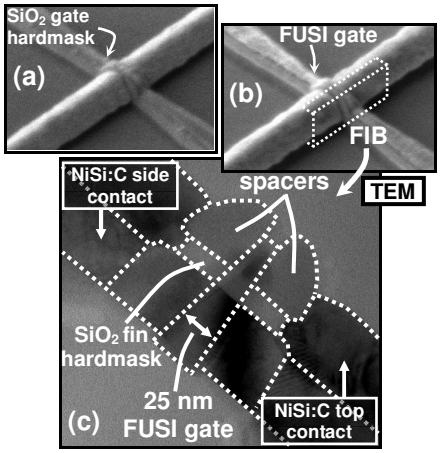

Fig. 5 Isometric-view SEM images showing (a) a poly-Si gate FinFET with HS NiSi:C contacts (poly-Si gate is capped by a gate hardmask), and (b) a FUSI gate FinFET with HS NiSi:C contacts. (c) TEM image of a device as shown in (b). One of the FUSI side-gates is captured within the FIB sample.

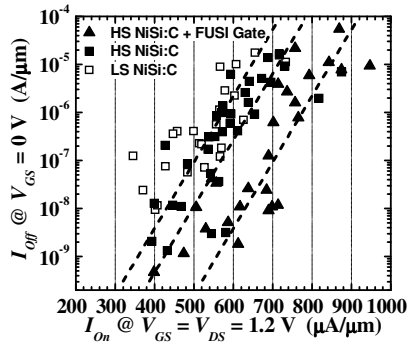

Fig. 6. I_{Off}-I_{on} plot showing ~14 % Ion enhancement of devices with HS NiSi:C contacts over devices with LS NiSi:C contacts at an I_{Off} of 1x10^{-7} A/µm. Integrating HS NiSi:C contacts with FUSI metal gate gives a combined enhancement of ~40 %.

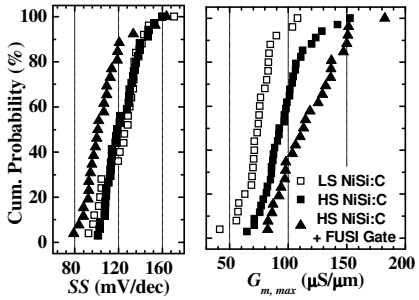

Fig. 7. Cumulative distributions of *SS* and G_m. of the same sets of devices used for the I_{Off}-I_{On} plot.

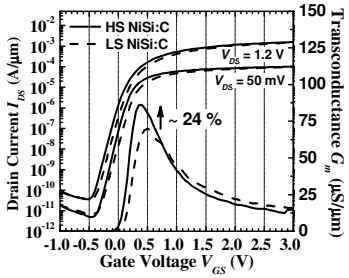

Fig. 8. I_{DS}-V_{GS} and G_m-V_{GS} characteristics of a pair of "LS NiSi:C" and "HS NiSi:C" devices.

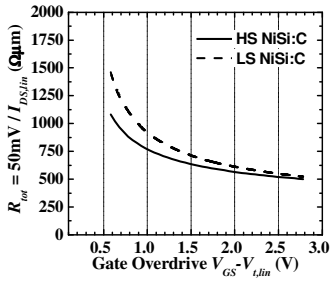

Fig. 9. S/D series resistance approximation using the asymptotic curve of R_{tot} versus V_{GS}-$V_{t,lin}$.

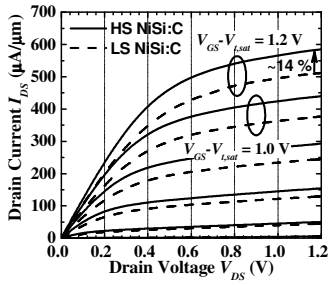

Fig. 10. I_{DS}-V_{DS} family of curves showing 14 % strain-induced I_{Dsat} enhancement at V_{GS}-$V_{t,sat}$ = 1.2 V, where $V_{t,sat}$ = V_{GS} at which I_{DS} = 1 x 10^{-7} A/µm when V_{DS} = 1.2 V.

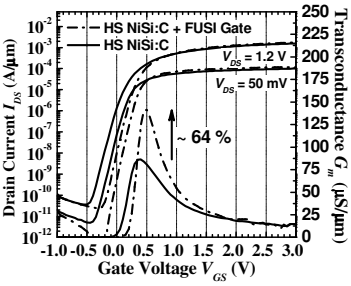

Fig. 11. I_{DS}-V_{GS} and G_m-V_{GS} characteristics of a pair of "HS NiSi:C" and "HS NiSi:C + FUSI gate" devices. With FUSI, gate stress effects and increase in C_{ox} results in significant peak G_m enhancement.

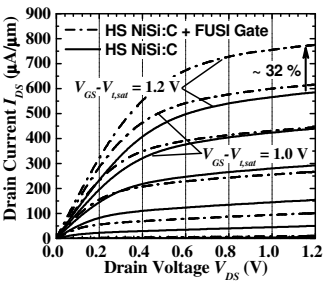

Fig. 12. Integration with a high-stress FUSI metal gate results in a further 32 % I_{Dsat} enhancement at V_{GS}-$V_{t,sat}$ = 1.2 V, where $V_{t,sat}$ = V_{GS} at which I_{DS} = 1 x 10^{-7} A/µm when V_{DS} = 1.2 V.