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Capacitive Parameter Extraction for Nanometer-Size Field-Effect Transistors

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1. Introduction

As the size of a field-effect transistor (FET) becomes smaller, it is increasingly difficult to evaluate small electrostatic capacitances in and around the device. Especially, gate-drain capacitance and that of a floating node are of interest, because the former greatly affects the high-frequency performance [1], and the latter is considered to limit the stability of circuit operation in the scaled-down LSI [2].

In this report, a simple test structure and evaluation method is proposed to extract atto-farad-order gate-drain capacitance, and the capacitances around a floating node between FETs.

2. Test Structure and Evaluation Method

Figure 1(a) shows the proposed test structure. Two FETs with a gate length of L and a width of W are serially connected, and the area between the two gates spaced by S becomes a floating node when both gates are turned off. The upper gate in a metal layer is necessary only when the capacitance between the floating node and the metal layer has to be evaluated. This kind of structure can readily be found in CMOS NAND and NOR gates [see Fig. 1(b)].

Capacitances are evaluated by measuring the transferred current I_d when gates are driven by high-frequency pulses shown in Fig. 1(c). Transferred charge Q in one pulse period is the difference between the amount of charge Q_2 in the floating node just after the lower gate 2 is turned off, and Q_1 just after the lower gate 1 is turned off (i.e. $Q=Q_2-Q_1$). Q_1 and Q_2 can be estimated based on the equivalent circuits shown in Fig. 2. C_{lg1}, C_{lg2}, C_{ug}, C_s, C_d and C_b are the capacitances between the floating node and lower gate 1, lower gate 2, upper gate, source, drain and substrate, respectively. V_{th1} and V_{th2} are the threshold voltages for lower gate 1 and 2. Based on the equivalent circuits, Q_1 and Q_2 can be expressed as

$$Q_1 = -C_d V_d - C_{ug} V_{ugH} - C_{lg1} V_{th1} - C_{lg2} V_{lg2L}, \text{ and}$$

$$Q_2 = \left(C_{lg1} + C_{lg2} + C_{ug} + C_b + C_s\right) V_d - C_{ug} V_{ugL} - C_{lg1} V_{lg1L} - C_{lg2} V_{th2}.$$

Because the floating node is raised to V_d before lower gate 2 is turned off [Fig. 2(b)], V_{th2} is also raised from the original V_{tho} roughly by V_d, whereas V_{th1} remains to be V_{tho}. Thus the transferred charge is calculated to be

$$Q = C_\Sigma' V_d + C_{ug} \Delta V_{ug} + C_{lg1}\left(V_{tho} - V_{lg1L}\right) + C_{lg2}\left(V_{lg2L} - V_{tho}\right)$$

where $C_\Sigma' = C_{lg1} + C_{ug} + C_b + C_s + C_d$, and

$$\Delta V_{ug} = V_{ugH} - V_{ugL}.$$

Considering that Q is I_d divided by pulse frequency f, we can obtain C_Σ', C_{ug}, C_{lg1} and C_{lg2} from I_d-V_d, I_d-ΔV_{ug}, I_d-V_{lg1L} and I_d-V_{lg2L} characteristics. Note that total capacitance around the floating node is not C_Σ', but $C_\Sigma'+C_{lg2}$.

3. Experiments

Fully depleted narrow-channel SOI MOSFETs [3] were evaluated by using the proposed method. Channel and active areas beside the gates are not intentionally doped, but the method is not limited to such devices.

Figure 3(a) shows the I_d-V_d characteristics for various f. The conductance of the device is exactly proportional to f, indicating that a fixed amount of charge is transferred in one period of the gate pulses. From the slope of conductance-frequency characteristics [Fig. 3(b)], we can see that C_Σ' is 45 aF.

Figure 4(a) shows the I_d-V_d characteristics for different ΔV_{ug}'s. These curves are parallel and equally spaced as expected from the theoretical estimation. From the I_d-ΔV_{ug} relationship at a fixed V_d [Fig. 4(b)], the ratio (slope) of 4.1 pS is obtained, and this gives a C_{ug} of 2.1 aF.

I_d-V_{lg1L} and I_d-V_{lg2L} characteristics at a fixed V_d are shown in Fig. 5. The former has a negative slope and the latter has a positive one as predicted, and from these, C_{lg1} and C_{lg2} of 30 aF are obtained.

The dependence of the above capacitive parameters on gate spacing S is shown in Fig. 6 for two gate oxide thicknesses t_{ox}. C_Σ' and C_{ug} increase with S, but C_{lg1} and C_{lg2} are almost constant. The thinner t_{ox} gives roughly 10-aF larger C_{lg1} and C_{lg2}, and this is directly reflected to C_Σ'.

These capacitive parameters are not sensitive to gate length L as shown in Fig. 7, indicating that the edge component is dominant in C_{lg1} and C_{lg2}, and C_Σ' and C_{ug} are mainly determined by S.

4. Conclusions

A simple test structure for extracting capacitive parameters in nanometer-size FETs is proposed, and high sensitivity in the order of atto farad is demonstrated by using narrow-channel SOI FETs. This method is especially useful in analyzing and optimizing the performance of the future scaled-down devices with complex structures.

Acknowledgements

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References

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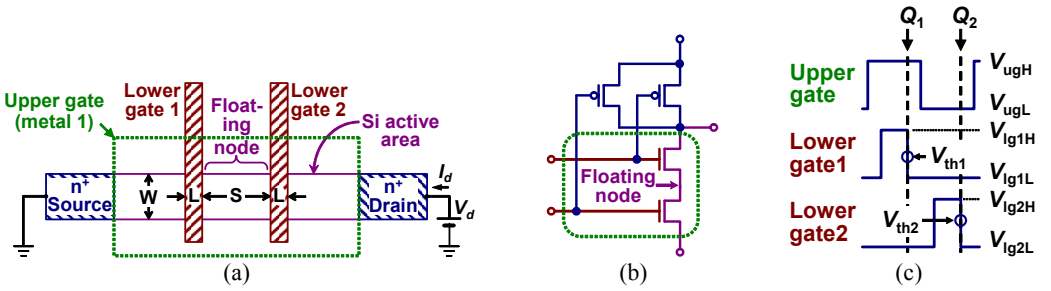

Fig. 1(a) A test structure for capacitive parameter extraction, (b) the structure found in a NAND gate, (c) waveforms of pulses applied to gate.

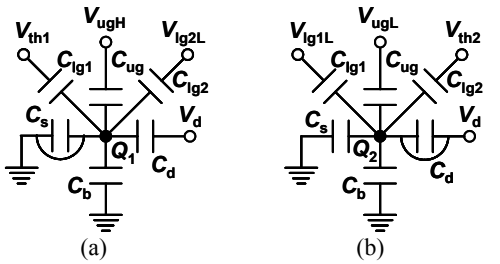

Fig. 2 Equivalent circuits to estimate the amount of charge Q_1 in the floating node just after the lower gate 1 is turned off (a), and Q_2 just after the lower gate 2 is turned off (b).

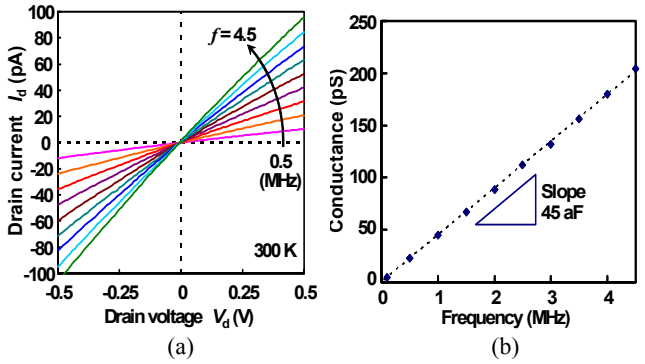

Fig. 3(a) I_d-V_d characteristics for various pulse frequencies for a device with L=300 nm, W=320 nm, S=300 nm and t_{ox}=5.0 nm. Measurement conditions are V_{lg1L}=V_{lg2L}=−1.8 V, V_{lg1H}=V_{lg2H}=1.8 V and V_{ugL}=V_{ugH}=7.5 V (ΔV_{ug}=0). (b) Conductance dI_d/dV_d vs. pulse frequency.

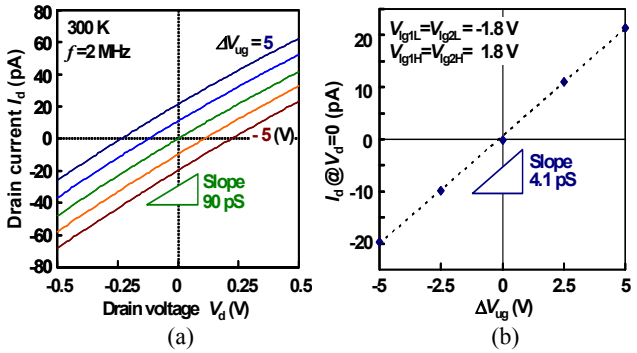

Fig. 4(a) I_d-V_d characteristics for various ΔV_{ug}'s (=V_{ugH}−V_{ugL}). (b) Zero-bias drain current vs. ΔV_{ug} for obtaining C_{ug}. The device and other conditions are the same as those in Fig. 3.

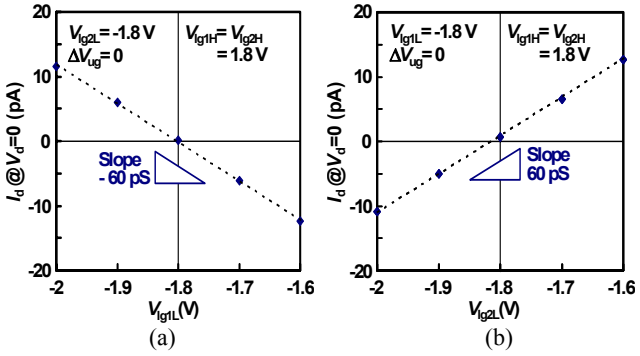

Fig. 5 Zero-bias drain current vs. V_{lg1L} (a) and V_{lg2L} (b) for obtaining C_{lg1} and C_{lg2}, respectively. The device and other conditions are the same as those in Fig. 3.

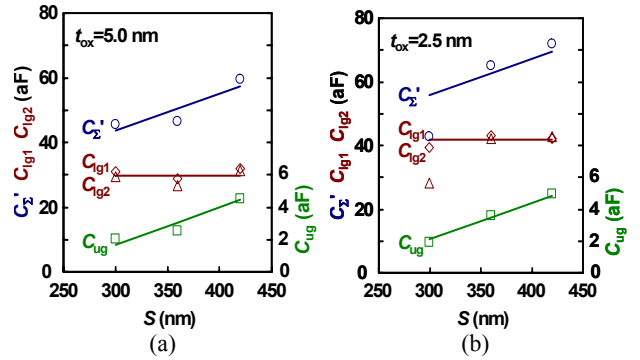

Fig. 6 Capacitive parameters C_Σ', C_{lg1}, C_{lg2} and C_{ug} as functions of gate spacing S for devices with t_{ox} of 5.0 nm (a) and 2.5 nm (b), L=140 nm and W=320 nm.

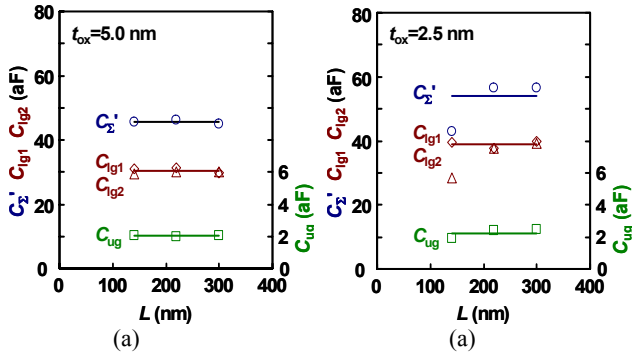

Fig. 7 Capacitive parameters C_Σ', C_{lg1}, C_{lg2} and C_{ug} as functions of gate length L for devices with t_{ox} of 5.0 nm (a) and 2.5 nm (b), W=320 nm and S=300 nm.