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Two-step Inverse Modeling for Estimation of Channel Impurity Pile-up

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1. Introduction

Optimization of channel impurity profile is essential to realize high performance MOSFETs with suppressed short channel effect. Although TCAD can calculate impurity profile, predictive calculation is difficult and calibration is required. Therefore, an evaluation method based on experimental measurements is important. Inverse modeling, i.e., adjusting impurity profile in device simulation to match simulation results with experimental electrical results [1, 2], is an effective way to know actual impurity profile.

In this work, we developed a new scheme of inverse modeling, focusing on the estimation of channel impurity pile-up. Impurity pile-up should be suppressed since high impurity concentration near the surface severely enhances Coulomb scattering and random variation of threshold voltage (V_{th}) [3]. It is helpful if the impurity pile-up can be estimated by electrical measurements. By taking drain induced barrier lowering (DIBL) into account, this scheme can estimate effective impurity profile in short channel devices, and thus can evaluate gate length (L_g) dependence of channel impurity pile-up. MOSFETs activated with spike anneal (SA) or non-melt laser anneal (LA) are evaluated and compared.

2. Evaluation Procedure

The impurity profile assumed for inverse modeling is shown in Fig.1. In the vertical direction, a profile with a uniform concentration at the deep region (conc.: N_{sub}) and a linear function near the surface (conc.: N_{pile}, depth: D_{pile}) is assumed. The surface terms represent impurity pile-up. It is assumed that the parameters are dependent on channel length due to the horizontal overlap of halo or pile-up, but lateral non-uniformity within a single transistor is ignored for simplicity. Since the number of parameters is only three per transistor, relationship between electrical characteristics and extracted profile is clear. This contributes to stable and fast extraction.

Experimentally measured V_{th} and subthreshold swing S as functions of substrate bias V_{sub} and drain voltage V_d are used for evaluating the impurity profile. Concept of the scheme is explained in Fig. 2. The evaluation procedure consists of two steps. At the 1st step, N_{sub} is adjusted to fit V_{th} shift due to V_{sub} change (ΔV_{th}-V_{sub}), V_{th} shift due to V_d change (ΔV_{th}-V_d), and S. At the 2nd step, N_{pile} and D_{pile} are adjusted to fit V_{th}. It is necessary to include ΔV_{th}-V_d (i.e. DIBL) to correctly reproduce the characteristics of short channel devices.

N_{sub} corresponds to effective impurity concentration regarding the body effect and DIBL. If experimental V_{th} is higher than that determined by N_{sub} value, it is considered that impurity concentration near the surface is higher than that at the depletion layer edge. This can be utilized to estimate the surface profile.

Actually, deep region is re-adjusted at the 2nd step in order to take the influence of surface concentration to depletion layer width into account. Besides, V_{th} itself is not used but L_g dependence of V_{th} (ΔV_{th}-L_g) is used at 2nd step in order to avoid being affected by any uncertainty of gate workfunction in device simulation and fixed charge. Thus L_g independent fixed amount of inaccuracy may exist in the estimated amount of pile-up. ENEXSS [4] is used for device simulation and inverse modeling.

3. Samples

LA is attracting much attention for device scaling since its diffusion-less and high-activation nature [5-8]. In this work, to confirm the usefulness of the developed scheme, two sets of nMOSFETs are evaluated as subjects: one is annealed by SA, and the other is annealed by LA [5]. Typically the SA condition was set to be 1030-1070℃ for a few seconds, and the LA was >1300℃ for <1 msec. L_g and halo dose are varied for each set. Effective doping concentration considering gate depletion is used for gate polysilicon, and Gaussian functions which approximate TCAD-predicted profile are used for source/drain region in device simulation for each set.

4. Results

Figure 3 shows experimentally measured V_{sub} and V_d dependence of V_{th}, which is used for inverse modeling. Figure 4(a) and (b) show both experimental and fitted V_{th} roll-off for SA and LA devices. Intermediate results (after 1st step) for SA devices are also shown. A large discrepancy in V_{th} arises when fitting is done based on V_{th} shift. Such a discrepancy also exists in LA devices, but it is smaller than in SA devices. This discrepancy diminishes with adding the surface terms and re-adjusting N_{sub}.

Figure 5(a) and (b) show estimated vertical impurity profile for several L_g's for SA and LA devices. In both cases, N_{sub} increases with decreasing L_g. This can be explained as an increase in effective doping due to halo overlap. The magnitude of surface terms is very large in SA devices, indicating very strong pile-up. Besides, it increases with decreasing L_g. On the other hand, the surface terms in LA devices are very weak, suggesting that LA devices are almost free from pile-up.

Figure 6(a) and (b) shows halo dose dependence of vertical impurity profile at L_g = 40 nm for SA and LA devices. Concentration at deep region increases with halo dose. The surface terms also increase with halo dose in SA devices, whereas the surface terms are very weak regardless of halo dose in LA devices. It is also noticed that the halo dose at deep region is weakened due to the redistribution in SA devices. Although the shapes of V_{th} roll-off is comparable (Fig. 4), impurity profile is considerably different in SA and LA devices. Such significant differences are attributable to difference in impurity redistribution during annealing, and the developed scheme can easily detect such process condition dependence.

5. Conclusion

A new scheme of inverse modeling for estimating channel impurity pile-up is developed. A significant difference in impurity profile between spike-annealed and laser-annealed devices was able to be detected. This scheme is stable and fast because of its simplicity, and is helpful for process optimization.

References

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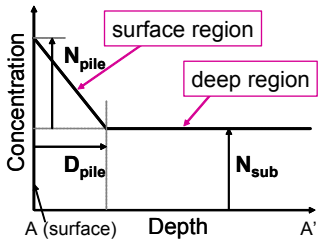

Fig. 1: Assumed simplified impurity profile for vertical direction (A-A' cross section in Fig. 2(b)). N_{sub} gives effective concentration regarding the body effect and the short channel effect. Surface terms (N_{pile} and D_{pile}) represent impurity pile-up.

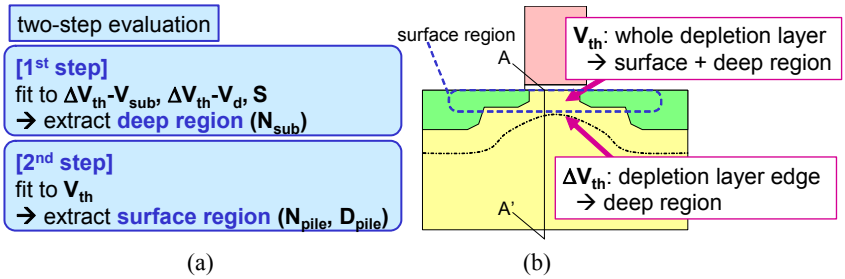

Fig. 2: Concept of two-step evaluation. (a) Evaluation steps. (b) Schematic cross section of a MOSFET indicating surface region and depletion layer edge. ΔV_{th}-V_{sub} and ΔV_{th}-V_d are mainly determined by depletion layer edge, and thus impurity profile at the deep region (which include depletion layer edge) can be extracted using ΔV_{th}. V_{th} is determined by whole depletion layer, and thus once the deep region has been fixed, the surface region can be extracted using V_{th}.

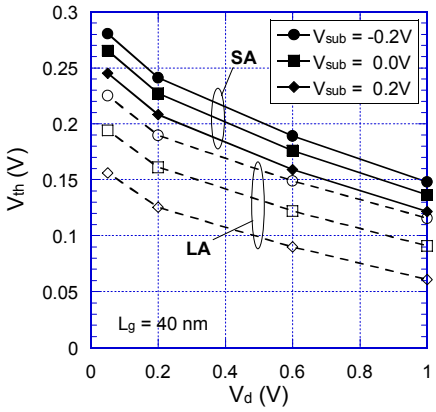

Fig. 3: Measured V_{sub} and V_d dependence of V_{th} for SA and LA device at L_g = 40 nm.

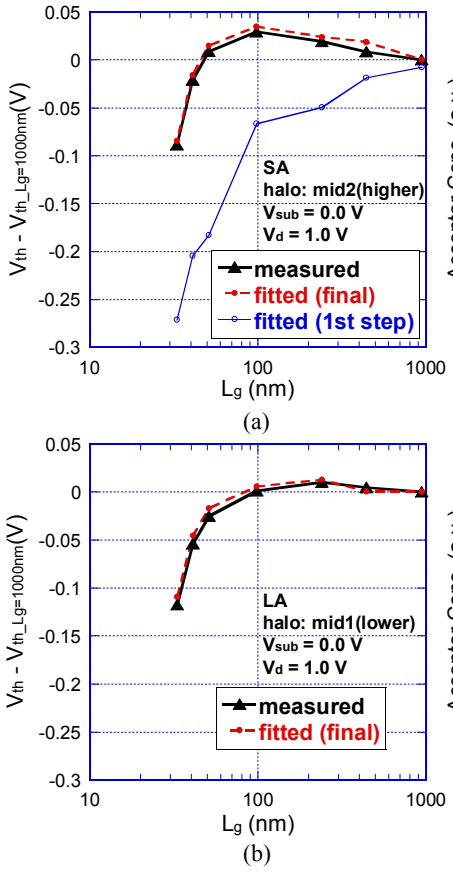

Fig. 4: Measured and fitted V_{th} roll-off for (a) SA and (b) LA devices at V_{sub} = 0.0 V and V_d = 1.0 V. Intermediate result (after 1st step) is also shown for SA.

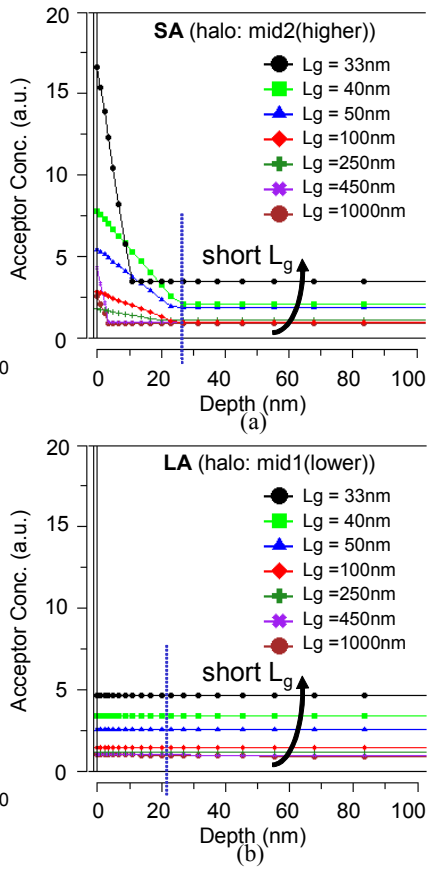

Fig. 5: Extracted effective impurity profile for vertical direction for different L_g's; (a) SA and (b) LA devices. Dotted lines show depletion layer width at L_g = 40 nm.

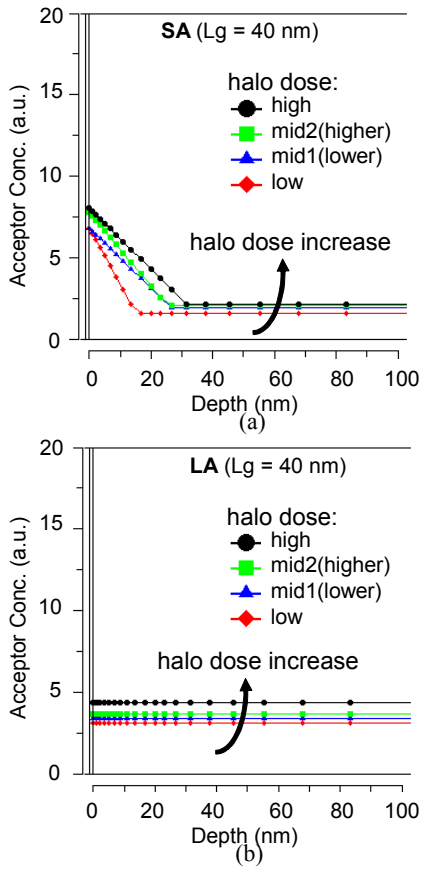

Fig. 6: Extracted effective impurity profile for vertical direction for different halo dose condition; (a) SA and (b) LA devices.