

## B-8-4

### Discrete-Dopant-Fluctuated Threshold Voltage Roll-Off in Sub-16nm Bulk FinFETs

Yiming Li\*, Chih-Hong Hwang, Hsuan-Ming Huang, and Ta-Ching Yeh

Department of Communication Engineering, National Chiao Tung University

\* Corresponding author. Address: P.O. Box 25-178, 1001 Ta-Hsueh Rd., Hsinchu 300, Taiwan  
TEL: +886-930330766; FAX: +886-3-5726639; and Email: ymli@faculty.nctu.edu.tw

#### 1. Introduction

As the dimension of semiconductor devices shrunk into nanometer scale, atomistic induced fluctuations of electrical characteristics are especially pronounced [1-6]. Nanoscale transistors with vertical channel structure, such as fin-typed field effect transistors (FinFETs) are promising candidates for next generation devices [5-8].

In this paper, we for the first time investigate the fluctuations of threshold voltage ( $V_{th}$ ) roll-off in nanoscale bulk FinFETs by a three-dimensional (3D) statistically full-scale “atomistic” device simulation technique. Discrete dopants have been statistically positioned in the 3D channel region to explore associated carrier transportation characteristics, concurrently capturing “dopant concentration variation” and “dopant position fluctuation”. The bulk FinFET significantly suppresses fluctuation of  $V_{th}$  roll-off; it merely has two fifths fluctuation, compared with planar nano-CMOS devices [4]. The S.D. of  $V_{th}$  is proportional to  $(WL)^{-0.75}$ , which is better than  $(WL)^{-0.5}$  of planar devices [2]. The superior immunity against fluctuation [5] and stable fluctuation of  $V_{th}$  roll-off imply the bulk FinFET is promising in sub-16nm era.

#### 2. Methodology and Results

All statistically generated discrete dopants, shown in Fig. 1, are incorporated into the large-scale 3D device simulation under parallel computing system [8]. The quantum mechanical transport simulation is performed by solving a set of 3D density-gradient equation coupling with Poisson equation and electron-hole current continuity equations [8]. This approach allows us to concurrently explore the fluctuations of electrical characteristics induced by the randomness of dopant number and position in the channel region. Figure 1(a) shows 5000 discrete dopants randomly distributed in  $(150\text{nm})^3$  cube with average concentration of  $1.48 \times 10^{18} \text{cm}^{-3}$ . The dopants may vary from 26 to 55, where the average number is 40, within its 125 sub-cubes of  $(30\text{nm})^3$ , as shown in Figs. 1(b) and 1(d), respectively. These 125 sub-cubes are then equivalently mapped into the FinFET’s channel region for the discrete dopant simulation, as shown in Fig. 1(c). Similar, discrete-dopant distributions for 22nm- and 16nm-gate are shown in Figs. 1(e) and 1(f).

Figure 2 shows the comparison of the normalized  $V_{th}$  and the  $V_{th}$  distribution for the 30nm-, 22nm-, and 16nm-gate bulk FinFETs, respectively. As device’s gate length scales down, the  $V_{th}$  scales with an increasing  $V_{th}$  fluctuation. From the random-dopant-number point of view, the equivalent channel doping concentration increases when the dopant number increases. It substantially alters the threshold voltage and the on- and off-state currents. On the other hand, even devices with the same dopants in the channel; the significant difference of  $V_{th}$  of these devices exhibits the effect of random-dopant-position-induced fluctuations. To explore the random-dopant-position induced  $V_{th}$  fluctuation, the on-state potential distributions of the 16nm bulk FinFETs with 6 discrete dopants inside channel (average concentration:  $1.48 \times 10^{18} \text{cm}^{-3}$ ) and the nominal case (i.e., the continuous dopant  $1.48 \times 10^{18} \text{cm}^{-3}$ ) are studied.

For device with a minimum  $V_{th}$  of the studied cases, the top-gate potential distribution near source side, shown in Fig. 3(c), is larger than the nominal case, shown in Fig. 3(a), due to the lack of discrete dopants located near the channel surface. On the other, for device with a maximum  $V_{th}$  of the studied cases, shown in Fig. 3(b), there are 5 dopants located near the channel. The potential distribution on top- and lateral-gates shows significant lower potential than other cases. The lower potential might impedes or change the electron flow path. Random-dopant-position induces different fluctuation of characteristics in spite of the same number of dopants. The results of the studied devices with equivalent doping concentration as  $1.48 \times 10^{18} \text{cm}^{-3}$  are summarized in Fig. 3(d). Figure 4 shows on/off-state current characteristic fluctuations. For cases with similar on-state current ( $I_{on}$ ), a maximum fluctuation of off-state current ( $I_{off}$ ) increases significantly as the gate length is scaled down. In addition, the spreading range of normalized  $I_{on}$  shows the magnitude of  $I_{on}$  fluctuations. The plot of  $V_{th}$  roll-off and standard deviation of  $V_{th}$  fluctuations in the 30nm-, 22nm-, and 16nm-gate length bulk-FinFETs are shown in Fig. 5. The standard deviation (S.D.) of  $V_{th}$  of the studied 30nm-gate device is 1.28 and 1.61 times smaller than 22nm- and 16nm-gate ones. Comparison of the S.D. of  $V_{th}$  between the bulk FinFETs and the planar MOSFETs [4] is shown in Fig. 6. As gate length scales from 30nm to 16nm, the fluctuation of  $V_{th}$  of the bulk FinFETs and planar devices increases 11mV and 27.3mV $^{-0.75}$ , respectively. The S.D. of  $V_{th}$  is proportional to  $(WL)^{-0.75}$ , which is better than  $(WL)^{-0.5}$  of planar MOSFETs. This result shows that the bulk FinFET exhibit a less fluctuation of  $V_{th}$  toll-off, two fifths times smaller, than planar ones for its better channel controllability.

#### 3. Conclusions

We have statistically explored the random dopant effects on the characteristics of the nanoscale bulk-FinFET using a full-scale 3D atomistic simulation technique. Our preliminary results show that the bulk FinFETs significantly suppress fluctuation of  $V_{th}$  roll-off (S.D. of  $V_{th} \sim (WL)^{-0.75}$ ); it only has two fifths fluctuation, compared with planar nano-CMOS devices. The stable and superior immunity against fluctuation [5] of  $V_{th}$  roll-off imply the bulk FinFET is promising in sub-16nm era.

#### Acknowledgement

This work was supported in part by Taiwan National Science Council (NSC) under Contract NSC-95-2221-E-009-336 and Contract NSC-95-2752-E-009-003-PAE, by MoEATU Program, Taiwan, under a 2006-2007 grant, and by the Taiwan Semiconductor Manufacturing Company under a 2006-2007 grant.

#### References

- [1] F.-L. Yang *et al.* in: Dig. Tech. Symp. VLSI Tech., to appear (2007).
- [2] F.-L. Yang *et al.* in: Proc. IEEE CICC, 691 (2006).
- [3] S. Roy *et al.* SCIENCE, **309** 388 (2005).
- [4] Y. Li *et al.* In: Proc. IEEE SNW, to appear (2007).
- [5] Y. Li *et al.* Microelec. Eng., to appear (2007).
- [6] Y. Li *et al.* Jpn. J. Appl. Phys., **45**, 6860 (2006).
- [7] Y. Li *et al.* in: Proc. IEEE Conf. Nanotech., **2**, 569 (2006).
- [8] Y. Li *et al.* IEEE Trans. Nanotech., **4**, 510 (2005).

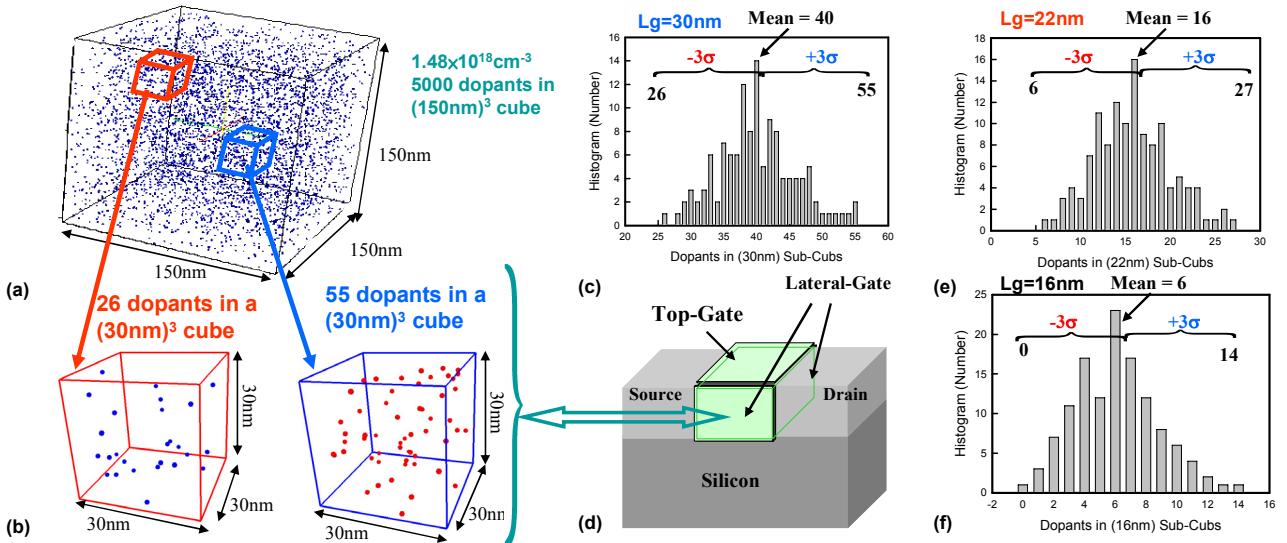


Figure 1. (a) Discrete dopants randomly distributed in  $(150\text{nm})^3$  cube with average concentration of  $1.48 \times 10^{18} \text{cm}^{-3}$ . There will be 5000 dopants within the cube, but dopants may vary from 26 to 55 (average number is 40) within its 125 sub-cubes of  $(30\text{nm})^3$ , ((b), and (d)). The 125 sub-cubes are then equivalently mapped into channel region for dopant position/number-sensitive simulation (c). Similar statistically generated discrete-dopant distributions for 22nm- and 16nm-gate length are shown in (e) and (f).

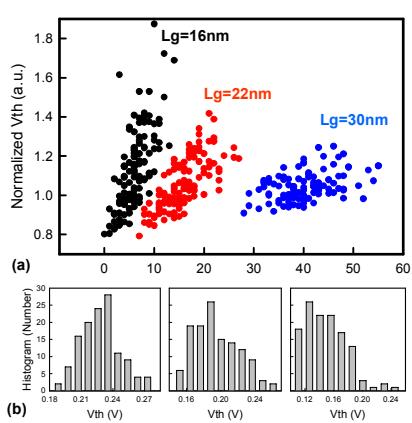


Figure 2. (a) Comparison of the normalized  $V_{th}$  and (b) the distribution of  $V_{th}$  for the 30nm-, 22nm-, and 16nm-gate devices.

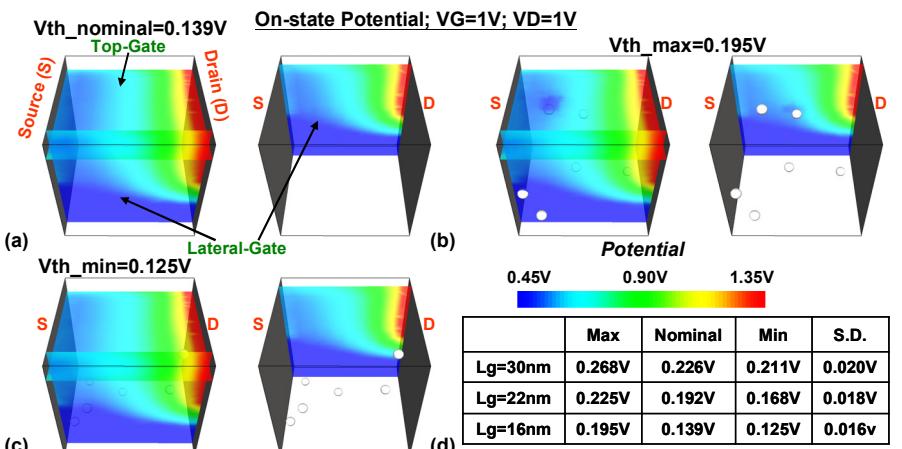


Figure 3. Plots of the on-state potential for the 16nm device with the same discrete dopant numbers (6 discrete dopants) but different  $V_{th}$  due to random dopant position. (a) The cross-sectional potential (extracted from the 2nm under top- and lateral-gates) of the nominal case ( $1.48 \times 10^{18} \text{cm}^{-3}$  doping concentration). The potentials for the device having (b) a maximum and (c) a minimum  $V_{th}$ . For device with different  $L_g$ , results of  $V_{th}$  and their standard deviations (S.D.s.) are summarized in (d).

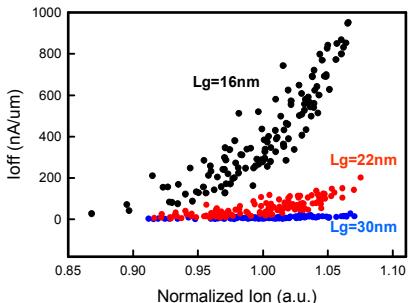


Figure 4. The on-off state current characteristics of the 30nm-, 22nm-, and 16nm-gate bulk FinFET devices.

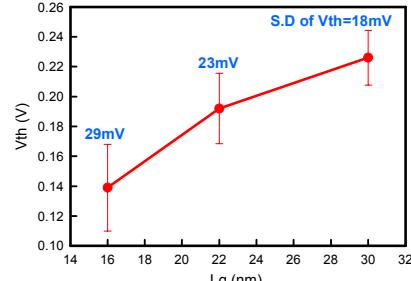


Figure 5. Plot of  $V_{th}$  roll-off for the 30nm-, 22nm-, and 16nm-gate bulk FinFETs, where the bars are the S.D. of  $V_{th}$ .

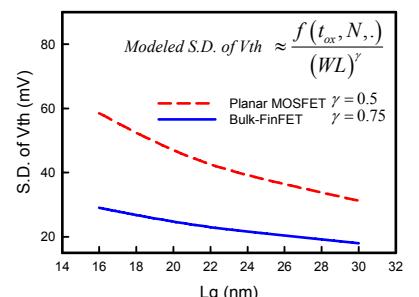


Figure 6. Comparison of the S.D. of  $V_{th}$  roll-off (i.e., versus the  $L_g$ ) of the bulk FinFETs and the planar MOSFETs [2,4].