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A Novel Embedded Extension SiGe (e^2SiGe) Process for PFET Performance Enhancement for 45nm Technology and beyond

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Abstract

We present for the first time an Embedded Extension SiGe (e^2SiGe) process that utilizes both the Extension (ext) and Source/Drain (S/D) regions to induce uniaxial strain to the Si channel formed using a novel RIE and single step SiGe epi process. This e^2SiGe process results in pFET performance gain of more than 25% over a typical eSiGe control that only has SiGe in the S/D. A combination of this e^2SiGe approach with a compressive stress liner (CSL), realized a high pFET drive current, I_{on}=800μA/μm, at off state current, I_{off}=100nA/μm, at V_{dd}=1V. (keywords: Unixial strain, e^2SiGe, Extension, Source/Drain)

Introduction

The scaling of CMOS has mainly being dominated by stress engineering for the past few years. In the case of pFET, the successful incorporation of CSL [1] and eSiGe in the S/D region [2] has improved the pFET performance tremendously.

In order to maximize the potential of SiGe stressor, comprehensive studies need to be carried out in terms of the integration schemes as well as the Ge concentration and position of the SiGe used. We have recently reported an early eSiGe integration scheme [3] whereby the SiGe module is inserted before the ext/halo implants. Due to the early insertion of the eSiGe module, this scheme requires careful implant damage optimization and thickness control for junction engineering as compared to a late eSiGe scheme.

As such, in this paper, a study on optimizing a late eSiGe integration scheme (i.e. eSiGe module inserted after ext/halo implant) is carried out. In addition, we also demonstrated for the first time a single step SiGe growth in the ext and S/D regions based on this integration scheme. This enables the closest proximity ever reported for SiGe stressor to induce strain on the channel without degrading parasitic and punch-through characteristics of the device. Table 1 shows that a competitive pFET performance has been achieved using e^2SiGe as compared to reports in the literature.

Experimental

The devices fabricated have Tox of 1.15nm, Lpoly: 35nm, W: 2um and measured at Vdd: 1V. The key process steps is reported in previous work [2, 5]. The main difference involves an optimized and well-tailored RIE process. This RIE process creates voids within the ext region as shown in Fig 1. The ability to manipulate the Si RIE plays a pivotal role in the subsequent positioning of the SiGe stressor. Fig 1 also shows the RIE that is able to remove the ext region symmetrically without affecting the surrounding Si and demonstrating the optimized RIE that has been achieved.

An optimized in-situ doped Boron selective epitaxial growth (SEG) is then carried out to completely fill the Si etch profile as shown in Fig 2. Note that the SiGe growth is "pinned" by the spacers and this creates a controllable thickness of SiGe growth in the ext region. This is important since either an over-fill or under-fill eSiGe would result in stress fluctuation. Fig. 3 compares a convention RIE profile and an aggressive isotropic S/D RIE profile. The process is completed with silicidation and stress liner formation before typical back-end processing.

Results and Discussions

Simulation result in Fig. 4 predicts that the device channel stress is enhanced for the case where ext region is filled with SiGe. In this case, 0% depicts no SiGe in the ext and 100% means the ext region is fully filled by SiGe. Fig. 4 also shows the channel stress monotonically increases as the SiGe is brought closer to the channel region.

Fig. 5 shows the pFET performance comparison of an optimized selective Si RIE using e^2SiGe process with (1) eSiGe in S/D region and (2) close eSiGe proximity achieved through aggressive isotropic RIE of the S/D profile shown in Fig. 3. It is noted that for the aggressive isotropic RIE, device punch-through is observed. This indicates the difficulty of achieving close proximity eSiGe profile merely by optimizing the proximity of the S/D RIE while maintaining good device characteristics in the late eSiGe flow. On the other hand, a pFET performance enhancement of 25% can be achieved using the e^2SiGe approach over devices with only eSiGe in S/D. This demonstrates the benefits of the presence of SiGe in the ext region as compared to typical isotropic S/D profile in terms of performance and punch-through characteristics.

Rodlin vs Lpoly plotted in Fig. 6 shows that mobility of the e^2SiGe process is greatly enhanced by ~60-70% as compared to control while the external resistance is increased. This agrees with simulation results that shows higher compressive stress gain with SiGe in ext. Furthermore, Fig. 7 shows that Vth roll-off characteristics of the e^2SiGe process is not degraded. Fig. 8 shows that the Vtsat-Isoff characteristics for e^2SiGe process is similar to eSiGe control. This suggests similar sub-threshold characteristics. Consistent 25% gain in Ion at same Vtsat is also demonstrated.

Normalized Cj and Cov data shown in Fig. 9 indicate no increase in junction capacitance increase with the new process. In addition, P+/NW junction leakage as shown in Fig. 10 is also found to be similar to the control sample. This indicates that the new e^2SiGe profile has negligible impact on device parasitic.

Conclusion

For the first time, a controllable and well-tailored RIE approach is successfully integrated in the process flow to realize an e^2SiGe profile that utilizes both the ext and S/D regions to induce strain on the Si channel. Without degradation in parasitic parameters, a high pFET I_{on}=800μA/μm, at I_{off}=100nA/μm, at V_{dd}=1V is achieved.

Acknowledgement

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Table 1: Comparison of this work with others works.

	This work	Ref 2	Ref 4	Ref 5	Ref 6	Ref 7
Gate stack	Poly-Si	Poly-Si	Poly-Si	Poly-Si	Poly-Si	NiSi
Lg (nm)	35	43	-	-	30	35
Tox (nm)	1.15	1.1	1.1	-	1.3	1.2
Vdd (V)	1.0	1.0	1.0	1.0	1.0	1.2
Ion (uA/um)	800	640	770	750	396	1060
Ioff (nA/um)	100	50	100	100	1	100

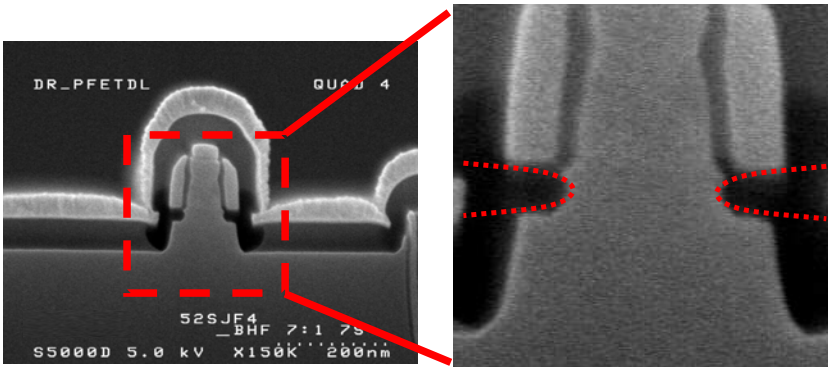

Fig 1: Cross sectional SEM of Si RIE resulting in voids in the extension region. Symmetric Si RIE profile has been achieved in both ext regions as shown in the right figure.

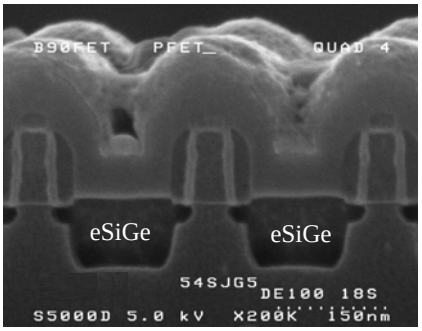

Fig 2: Cross-sectional SEM showing SiGe within the ext and S/D region and forms **E**mbedded **E**xtension **Si-Ge** (e^2-SiGe). Note that SiGe in ext is "pinned" by initial spacer

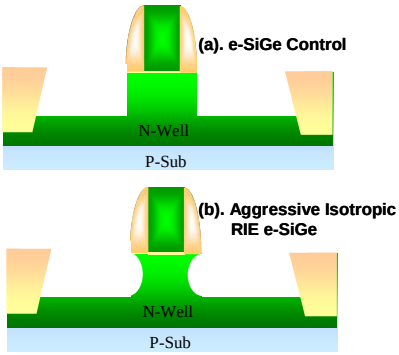

Fig 3: Two additional RIE profiles were created to compare with the e^2-SiGe which (a) depicts the control RIE and (b) uses an aggressive isotropic RIE to define Si-Ge

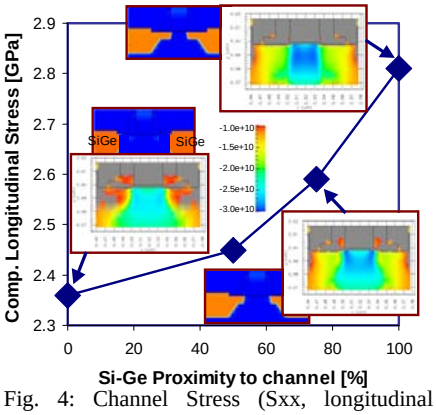

Fig. 4: Channel Stress (Sxx, longitudinal direction) vs percentage of Si-Ge proximity to Si channel.

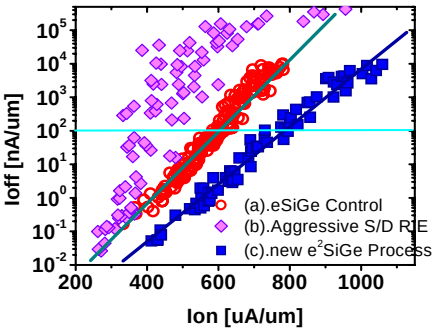

Fig. 5: PFET gain of 25% for e^2SiGe Process over eSiGe Control. Aggressive S/D RIE results in punch-through characteristics

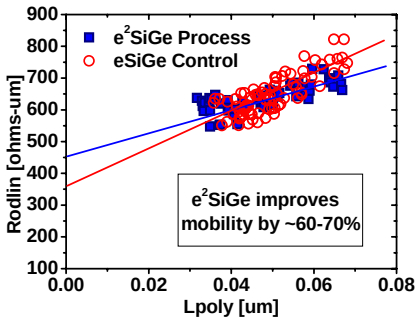

Fig. 6: Rodlin vs Lpoly comparison between e^2SiGe Process vs eSiGe Control. Mobility gain improvement of 60% is observed.

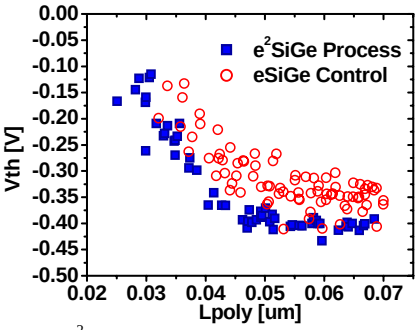

Fig. 7: e^2SiGe Process has comparable eSiGe Vt roll-off as compared to eSiGe control.

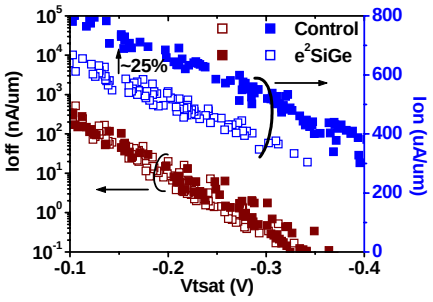

Fig. 8: Vtsat-Isoff and Vtsat-Ion relationship comparison between control and e^2SiGe Process. Comparable Vtsat-Isoff suggests similar sub-threshold characteristics.

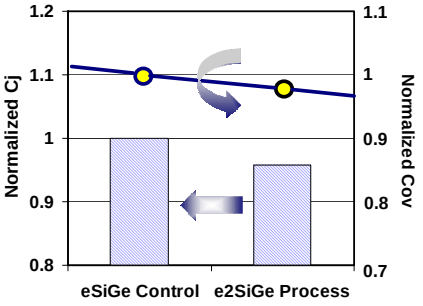

Fig. 9: Normalized junction capacitance and Coverlap shows e^2SiGe Process has slightly lower Cj and Cov.

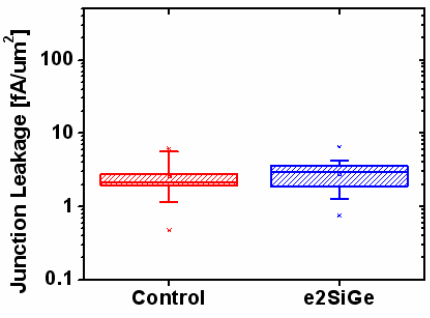

Fig. 10: P+/NW Junction leakage shows that e^2SiGe Process does not result in additional leakage currents.