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Wide-Range V_{th} Controllable SOTB (Silicon on Thin BOX) Integrated with Bulk CMOS Featuring Fully Silicided NiSi Gate Electrode

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1. Introduction

The demand for reducing the power consumption of system LSI chips is increasing. Variability of device characteristics has, however, been widely recognized as a major obstacle to improving performance per power-ratio beyond 45 nm generation. We proposed a fully depleted silicon-on-insulator (FD-SOI) MOSFET with an ultrathin buried oxide (BOX), named SOTB (Silicon on Thin BOX) as a solution to this problem [1]. The SOTB has been attracting much attention because of its wide-range back-gate controllability, which enables optimization both in performance and power [2-4]. In addition, the device, with a lightly doped thin SOI channel and a heavily doped substrate, has high immunity from short-channel effect and V_{th} fluctuation. We have shown, by simulation, that this device is robust against both dimensional and numeral fluctuations of dopant [5]. However, conventional poly-Si gate devices with a low doped channel cannot be used for low stand-by power (LSTP) applications due to their low V_{th}. In this paper, we developed a single FUSI (fully silicided) NiSi gate process to achieve the desired V_{th} for LSTP applications. Moreover, we integrated bulk transistors for high-voltage I/O operation by removing the thin SOI/BOX layers. We demonstrated the back-gate bias control of the SOTB and the characteristics of the integrated bulk transistors.

2. Device Fabrication and Results

A cross-sectional view of the SOTB/bulk hybrid structure is shown in Fig. 1. Advantages of this structure are summarized in the figure caption. The SOTB MOSFET with the well contact formed through the BOX layer enables back-gate control. At the same time, the low step height of the thin SOI/BOX layers means that bulk transistors can be easily integrated. This hybrid process flow is shown in Fig. 2. After shallow-trench isolation (STI) formation, the SOI layers (T_{SOI} = 15 nm) on both the well contact and bulk active regions were removed with a dry etching using a BOX layer (T_{BOX} = 10 nm) as a stopper, followed by removal of the BOX layer. Due to the low step height, gate patterning can easily be performed on both the SOI region and bulk region, as shown in Fig. 3. This process enables the fabrication of the SOTB/bulk hybrid structure without requiring epitaxial growth to reduce the height difference [6].

In the SOTB MOSFETs with a SiON gate dielectric (EOT = 1.9 nm), the elevated source/drain structure fabricated using Si selective epitaxial growth was adopted to reduce parasitic resistance. To prevent recesses in the SOI, conditions of gate- and sidewall- etching and precleaning before epitaxy were carefully optimized, resulting in a low external resistance (R_{sd} = 190 Ωμm) for 45-nm-gate-length NMOS, as shown in Fig. 4. When fabricating the FUSI gate, the gate poly-Si and the source/drain epitaxial Si were set to the optimal heights and silicided simultaneously in a single step, as shown in Fig. 5.

The subthreshold characteristics of the 45-nm-gate-length SOTB MOSFETs are shown in Fig. 6. FUSI gate devices have higher V_{th} and a suppressed short-channel effect, even with no increase in channel doping that may cause an increase in the variation in device characteristics. The I_{on} - I_{off} characteristics and the I_{on} - V_{th} relationships at V_{dd} = 1.2 V are shown in Figs. 7 and 8. Comparing FUSI gate devices with that of poly-Si gate ones at the V_{th} suitable for LSTP applications, higher I_{on} were achieved by suppressing gate depletion. The wide-range V_{th} control achieved by back-gate bias (V_{BG}) is demonstrated in Figs. 9 and 10. In the SOTB MOSFETs, we can control the central V_{th} values by well doping and selecting a FUSI or poly-Si gate. The time-to-time or area-to-area V_{th} can be controlled using the back-gate bias. By applying a reverse back-gate bias, the off drain currents can be reduced. In FUSI gate nMOS, the gate induced drain leakage (GIDL) current must be decreased to further reduce I_{off}. In addition, by applying a forward bias of 1.2 V, the drive currents of FUSI gate devices can be increased by 53% for NMOS and 43% for PMOS, while the BOX layer prevents any increase in leakage currents from the drain to the substrate. It should be noted that a forward bias higher than 0.6 V can never be applied in conventional bulk transistor structures. We demonstrated V_{th} controlability and reduction in V_{th} variation by applying a back-gate bias, as shown in Fig. 10. In cases where the fabricated devices have large V_{th} variations due to gate length or to channel dose fluctuations, we can set V_{th} to within a range of 180 mV and suppress standard deviation values σV_{th} to 1/4 using a 0.2 V step V_{BG} control.

At the same time as SOTB MOSFET fabrication, the I/O transistor was fabricated in the integrated bulk region. The desired values of V_{th} for the I/O transistor (V_{dd} = 3.3 V) were obtained using the NiSi gate with a lightly doped channel. Mobilities of hybrid bulk transistors are shown in Fig. 11. Carrier mobilities as high as universal curve were achieved for both FUSI and poly-Si devices with no sacrificial oxidation of the surface, indicating that little damage was caused by dry etching during BOX removal. The subthreshold characteristics at V_{dd} = 3.3 V of FUSI gate devices are shown in Fig. 12. The characteristics of the hybrid bulk transistor were comparable to those of a conventional bulk transistor, without any increase in leakage currents. TDDB results are shown in Fig. 13. The sufficiently long lifetime of the device is obtained at V_g = -3.3 V.

3. Conclusions

A simple FUSI NiSi gate process and hybrid SOTB/bulk CMOS integration have been developed using an ultrathin SOI/BOX substrate. We achieved the optimal V_{th} for LSTP applications in FUSI gate SOTB MOSFETs. We have shown that SOTB has wide-range V_{th} controllability using the back-gate bias, even with a gate length of around 45 nm. The characteristics of the integrated hybrid bulk transistor are comparable to those of conventional bulk transistors.

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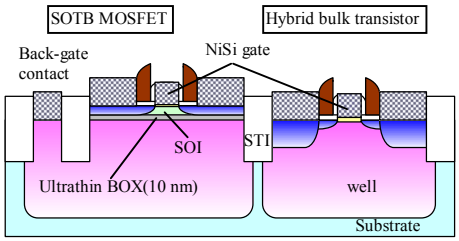


Advantages of the hybrid SOTB/bulk structure
-Back-gate bias control capable
-Reducing performance variation by trimming V_{th} values after fabrication
-High SCE immunity due to substrate (not SOI) doping
-Single NiSi gate (dual metal gate unnecessary)
-V_{th} control in FD-SOI (higher V_{th} than poly)
-Suppressing gate depletion (higher I_{on})
-Ultra low-dose channel
-Less V_{th} sensitivity to SOI thickness variation
-Reduction of V_{th} fluctuation due to dopant distribution
-No need to change the design for peripheral circuits

Fig. 1 Schematic cross-sectional view and device concepts of a hybrid SOTB/bulk structure.

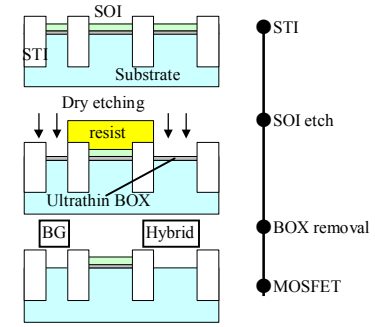


Fig. 2 Process flow of hybrid bulk fabrication.

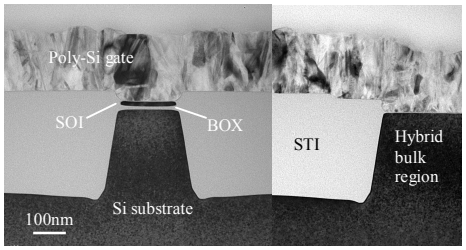


Fig. 3 A cross-sectional TEM image of poly-Si gate on the hybrid SOI/bulk regions.

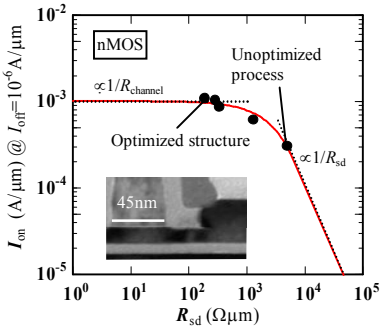


Fig. 4 The relationship between I_{on} and R_{sd}. R_{sd} greatly improved by optimized Si epitaxy.

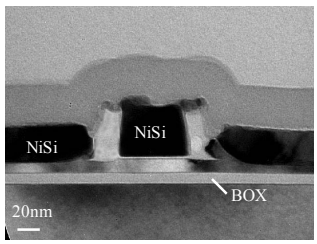


Fig. 5 A cross-sectional TEM image of FUSI gate SOTB MOSFET. The gate and the S/D were simultaneously silicided.

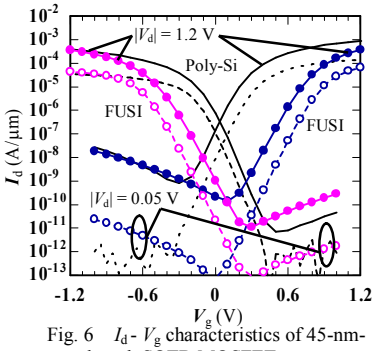
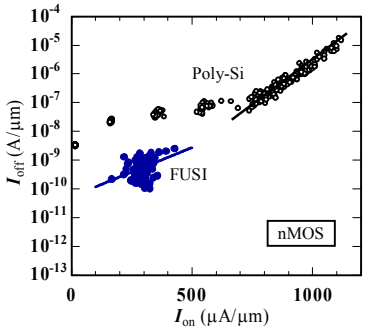


Fig. 6 I_d - V_g characteristics of 45-nm-gate-length SOTB MOSFETs.



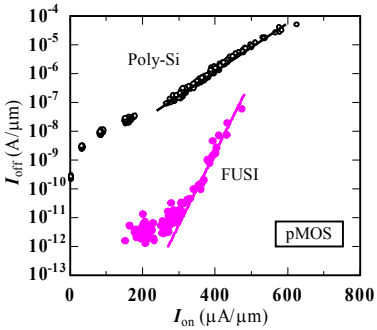


Fig. 7 I_{on} - I_{off} characteristics of SOTB MOSFETs at 1.2 V operation.

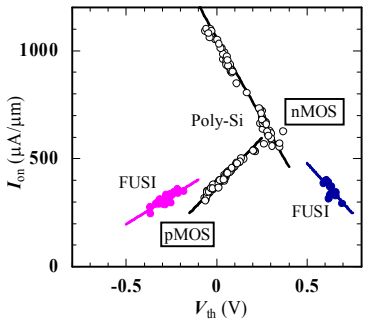


Fig. 8 I_{on} - V_{th} relationships of 45-nm-gate-length SOTB MOSFETs at 1.2 V operation.

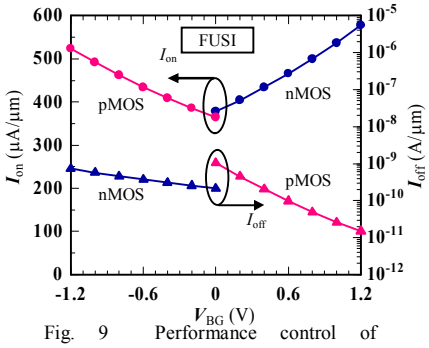


Fig. 9 Performance control of 45-nm-gate-length SOTB MOSFETs using back-gate bias at 1.2 V operation.

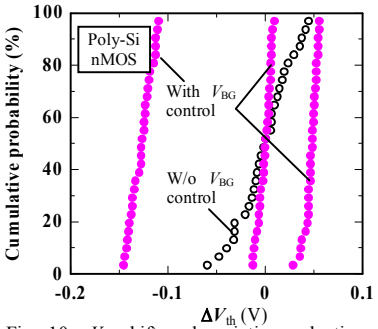


Fig. 10 V_{th} shift and variation reduction of 45-nm-gate-length SOTB using back-gate bias (V_{BG}:1.2 V ≥ V_{BG} ≥ -1.2 V, step = 0.2 V).

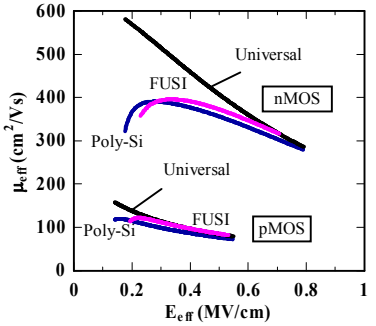


Fig. 11 Mobilities of hybrid bulk trs. No degradation was seen, that is, universal mobility was achieved.

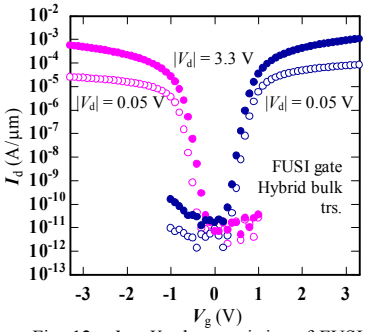


Fig. 12 I_d - V_g characteristics of FUSI gate hybrid bulk transitors at 3.3 V operation.

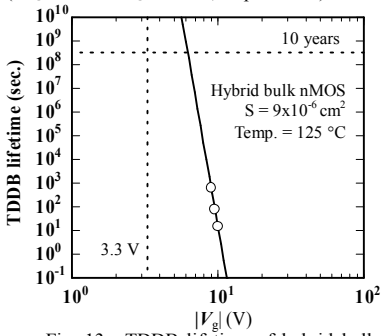


Fig. 13 TDDB lifetime of hybrid bulk transistor.