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Additivity between sSOI- and CESL-induced nMOSFETs Performance Boosts

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Abstract

We integrated both strained Silicon On Insulator (sSOI) substrates and highly-stressed Contact Etch Stop Layer (CESL) in Fully Depleted (FD)SOI nMOSFETs for gate length (L_G) down to 25nm and width (W) down to 50nm. More than 35% I_{ON} improvements were obtained due to the combination of sSOI and CESL. Thanks to extended characterizations and accurate extractions of the short channel mobility, we highlight and quantify the additivity of both "mobility boosters" for different channel widths.

Introduction

sSOI was already integrated as a channel material for Fully Depleted n and pMOSFETs [1] and its performance were compared with CESL ones [2]. In with work, we study the additivity of both sSOI- and CESL-induced performance improvements for short (L_G=25nm) and narrow (W=50nm) devices. Electrical characterisations have been carried out to extract the most important intrinsic parameters: the short channel effective mobility (μ_{eff}) and the parasitic series resistance (R_{series}).

Experiment description

sSOI have been elaborated using $Si_{0.8}Ge_{0.2}$ virtual substrates as templates. The final biaxial tensile strain in the sSi layer has been measured at 1.3 GPa. sSOI and conventional SOI wafers (all (100) oriented) have then been thinned down to T_{Si}=9nm and integrated with the FDSOI CMOS process described in [3] (with TiN/HfO_2, EOT=16.9Å, see Fig. 1). E-beam lithography has been used to get a L_m=40nm minimum "mask gate length". Then an oxide hard mask have been 15nm trimmed in order to obtain a L_G=25nm minimum physical gate length. 100nm thick 900MPa tensile ("t-CESL") or -2.2GPa compressive ("c-CESL") SiN CESL have been used on some SOI and sSOI wafers.

To extract the short channel mobility, we have measured the total resistance ($R_{tot}=V_d/I_{d,lin}$) at V_d=50mV for different gate lengths. This resistance is the sum of the parasitic series resistance (R_{series}) and the channel resistance (R_{ch}), this latter being proportional to $1/\mu_{eff}$: $R_{tot}=R_{series}+R_{ch}$ It is now widely accepted that the mobility generally depends on the gate length [4-5], even in undoped FDSOI channels [6-7]. That is why R_{tot} is generally not perfectly linear vs. L_G. However, locally (i.e. in a range of L_G where the mobility can be considered as constant), the short channel mobility can be extracted through the slope of $R_{tot}(L)$ [5]. That is the method we have used to get μ_{eff} for different gate voltage overdrives and consequently for different inversion charges, using $N_{inv}=C_{ox}(V_G-V_T)$. C_{ox} is measured on long and wide transistors and supposed as independent of the feature sizes and V_T is measured at a constant current (10^{-7} W/L_G). In most of our extractions, the range of L_G where parameters were extracted by the linear fitting of the $R_{tot}(L_G)$ is: 25nm<L_G<55nm (this detail is given on each figure). With this method, the parasitic source/drain resistance is given by $R_{tot}(L_{eff}=0)$. However, L_{eff} is difficult to extract. Capacitance measurements probably provide the more accurate values of L_{eff} [4]. However, it supposes that the gate to channel capacitance does not depend on the gate length. This assumption is not always true in advanced technologies [3]. That is why, in this work, we only comment on $R_{tot}(L_m=0)$ as a figure of merit of the extreme scalability. This value must be close to R_{series}, however.

Electrical results

Fig. 2 shows the I_{ON}-I_{OFF} for wide nMOS along the <110> direction. sSOI yields a 30% I_{ON}-I_{OFF} improvement at I_{OFF}=10nA/µm. This is due to a 80% enhancement of the low-V_D short channel mobility (Fig. 4), clearly evidenced by the sSOI-related lower slope of the $R_{tot}(L_m)$ in Fig. 3. It must be pointed out that $R_{tot}(L_m=0)$ is the same for SOI and sSOI (Fig. 5), suggesting that R_{series} are similar.

As far as CESL is concerned, compressive (tensile, respectively) layers degrade (improve, respectively) the short channel electron mobility (Fig. 4). This explains the t-CESL induced I_{ON}-I_{OFF} improvement in Fig. 2. However, this figure also shows that c-CESLs do not degrade nMOS current. This is due to the mobility reduction with c-CESL which is counteracted by a 30% R_{series} reduction, as evidenced in Figs 3 and 5.

This cCESL-induced R_{series} improvement happens even in narrow devices (Fig. 8), and quite independently of the channel direction (Fig. 11). So, the performance differences observed between wide <110>-oriented (Fig. 2), narrow <110>-oriented (Fig. 6) and narrow <100>-oriented devices (Fig. 7) rather come from the mobility dependence on the channel width and orientation. First, when the channel is narrower and narrower, the tCESLs become more effective than sSOI to boost the channel mobility (please compare Figs. 4 and 9). This must be due both to the t-CESL induced tension along the width direction, which is beneficial for nMOS, and, on the contrary, to the relaxation of the sSOI stress in this direction for narrow devices [1].

When the device directions change from <110> to <100>, both the sSOI and tCESL efficiency reduce (Figs. 6-7) because of a lower mobility improvement (Figs. 9-10). That shifts all the sSOI and tCESL related I_{ON}-I_{OFF} tradeoffs (full symbols in Figs. 9-10) to the left. In particular, the mobility enhancement due to tCESL lowers from 150% (155% with sSOI) in the <110> direction down to 36% (48% with sSOI) along the <100> direction. This might be explained by the tCESL-induced tension stress along the width direction, which is more beneficial along <110> for nMOSFETs.

Discussion

In the previous part, we demonstrate that cCESL reduces the parasitic source/drain resistance (this was confirmed by another extraction method [8]), that largely impacts the I_{ON}-I_{OFF} tradeoff. We speculate that the cCESL-induced tension in the source/drain region under cCESL (white arrows in Fig. 12) improves the electron mobility and, in turn reduces R_{series} on SOI (Figs. 5,8,11).

As far as the addition of CESLs and wafer level stress are concerned, for "low" stress levels, performance improvement can be cumulated (see the I_{ON}-I_{OFF} plots of Figs. 2,7 or the mobilities in Figs. 4,10). For "higher" stress levels, the performance improvement saturates at about 150% mobility- and 100% I_{ON}-improvements (Figs. 6 and 9). Finally, this work demonstrates that, in most cases (for mobility enhancement below 150%), sSOI and CESL and additive. Their performance boost can be fully added.

Conclusion

We explained the nMOSFETs performance with CESL and sSOI thanks to the extracted short channel mobility and parasitic source drain resistance down to L_G=25nm and W=50nm.We proved that their performance boosts can be added.

Acknowledgements

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References

[1] F. Andrieu et al, VLSI Tech., p. 134, 2006. [2] F. Andrieu et al, to be presented at VLSI Tech., 2007. [3] F. Andrieu et al., IEDM Tech. Dig., p. 641, 2006. [4] K. Romanjek et al., IEEE EDL 25, 8, p. 583, 2004. [5] K. Rim et al., IEDM Tech. Dig., p. 43, 2002. [6] F. Andrieu et al., IEEE SOI Conf., p. 223, 2005. [7] A. Cros et al., IEDM Tech. Dig., p. 663, 2006. [8] G. Ghibaudo et al., EL 24, 9, p. 543, 1988.

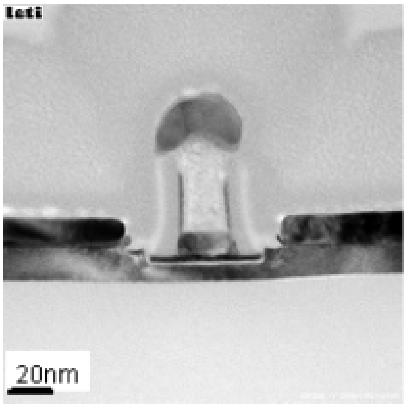

Fig. 1: TEM pictures of 25nm short devices with c-CESL and TiN/HfO_2 (T_{Si}=9nm).

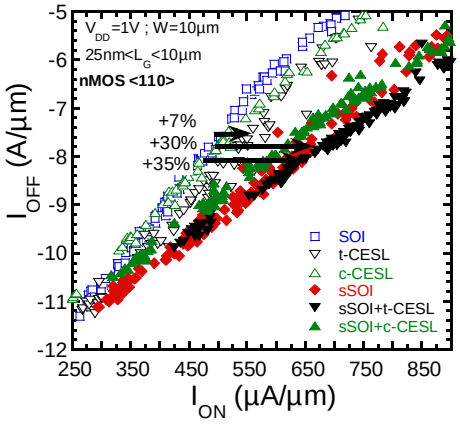

Fig. 2: I_{ON}-I_{OFF} for the different splits for nMOS.

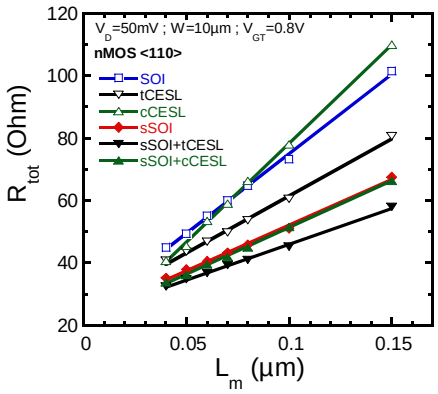

Fig. 3: $R_{tot}(L_m)$ for the different splits at V_G-V_T=0.8V for nMOS.

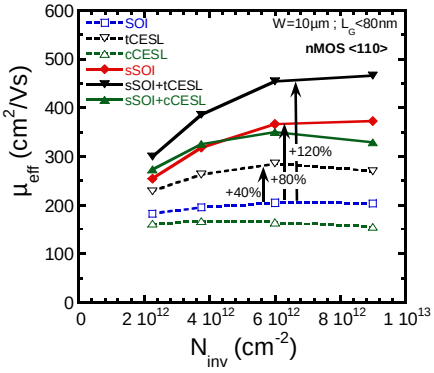

Fig. 4: Short channel electron mobility vs. inversion charge for the different splits.

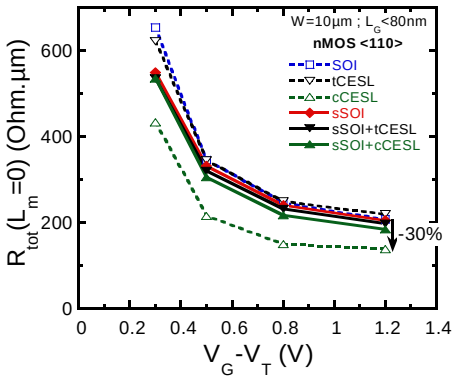

Fig. 5: R_{tot} at L_m=0 for short and wide (W=10µm) nMOSFETs.

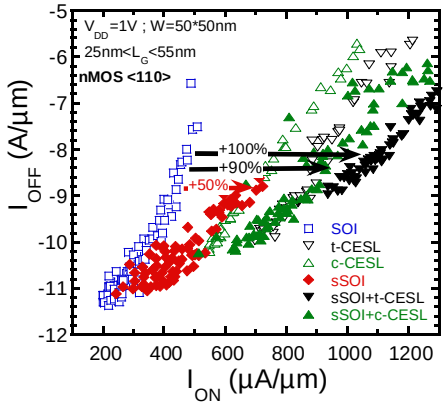

Fig. 6: I_{ON}-I_{OFF} for short and narrow nMOSFETs along <110>.

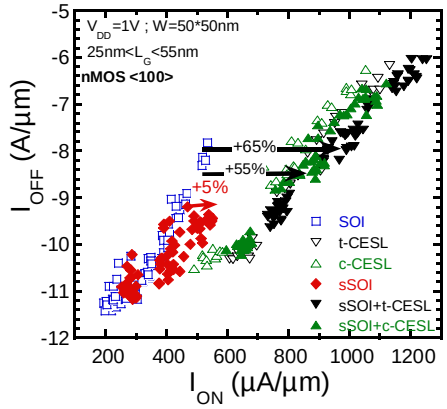

Fig. 7: I_{ON}-I_{OFF} for short and narrow nMOSFETs along <100>.

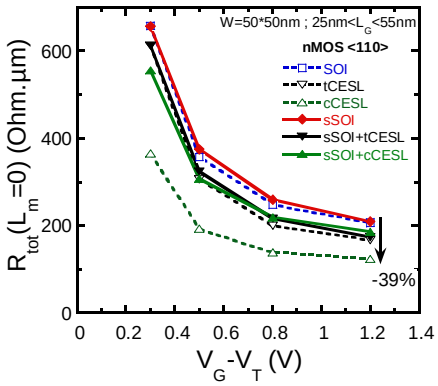

Fig. 8: R_{tot} at L_m=0 for short and narrow (W=50nm) nMOSFETs along <110>.

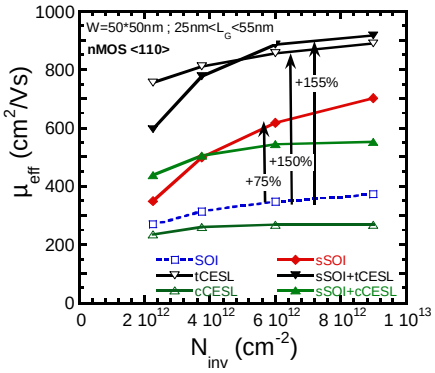

Fig. 9: Short and narrow channel electron mobility vs. inversion charge along <110>.

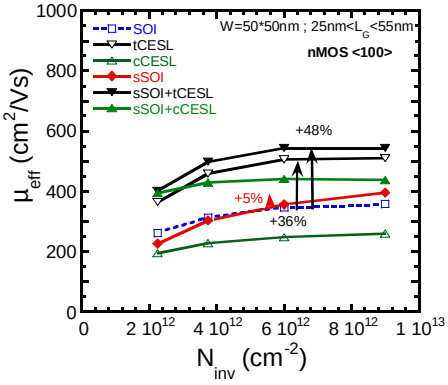

Fig. 10: Short and narrow channel electron mobility vs. inversion charge along <100>.

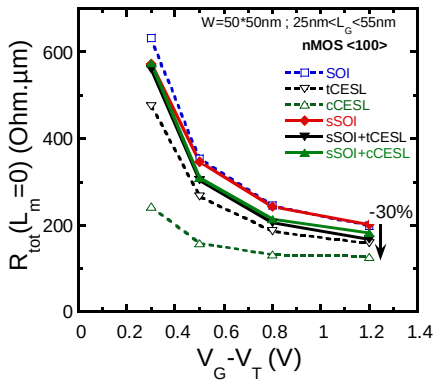

Fig. 11: R_{tot} at L_m=0 for short and narrow (W=50nm) nMOSFETs along <100>.

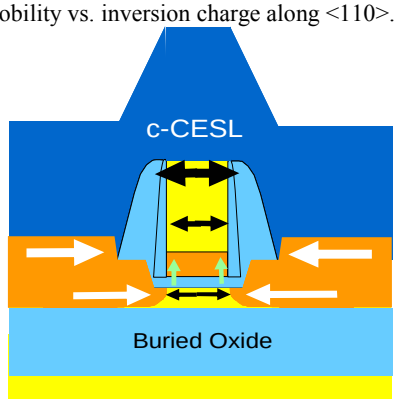

Fig. 12: Scheme of the different stress transfers from to cCESL to the channel.