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Novel Extended-Pi Shaped Silicon-Germanium (*e*Π-SiGe) Source/Drain Stressors for Strain and Performance Enhancement in P-Channel FinFETs

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1. INTRODUCTION

Mulitple-gate transistors or FinFETs offer excellent scalability beyond the 32 nm technology node. Strain engineering in FinFETs [1]-[3] is required to realize high performance levels commensurate with those of advanced planar FETs. Strained p-channel FinFETs with $Si_{0.8}Ge_{0.2}$ source/drain (S/D) stressors formed on the top surface of the Si fin have been reported [3]. To better exploit the strain effects, the SiGe S/D stressor has to be grown on the fin sidewalls as well, forming a Π-shaped S/D stressor [1]-[2]. Nevertheless, even for fins stressed by the Π-shaped S/D, the stress distribution in the Si fin still shows lower stress at the foot of the fin due to limited SiGe growth (geometrical effects on epitaxial growth) or stressor volume, and the non-compliance of the buried oxide (BOX).

In this work, we report a novel extended-Pi SiGe (*e*Π-SiGe) S/D stressor with significantly enhanced strain effects to boost the performance of p-channel FinFETs. Compared to FinFETs with Π-shaped SiGe S/D, FinFETs with the *e*Π-SiGe S/D have higher strain in the fin channel, leading to further performance improvement without any additional cost or process complexity.

2. DEVICE FABRICATION

The process flow for the fabrication of p-channel FinFETs with *e*Π-SiGe S/D is detailed in Fig. 1. 8" silicon-on-insulator (SOI) substrates with 30 nm thick Si were used. After threshold voltage V_t adjust implant, 248 nm lithography with phase-shift mask, resist trimming, and reactive ion etching were used to define Si fins with fin widths W_{fin} down to 60 nm. SiO_2 gate dielectric (~3 nm) was then thermally grown, followed by poly-Si gate deposition, gate pre-doping, gate definition, and etch. S/D extension implantation was performed. In the spacer formation process, SiN stringers at the base of the fins were removed to enable epitaxial growth of SiGe on the fin sidewalls. If the SiN stringers were not removed, SiGe S/D can only grow on the top surface of the fin [Fig. 2(a)] [3] and severely limit strain effects which is undesirable.

An extended pre-epitaxy clean was performed for the device in which FinFETs with *e*Π-SiGe S/D will be formed. The extended HF clean formed a recess in the buried oxide prior to the epitaxy step, exposing a portion of the bottom surface of the fin. Selective epitaxial growth of $Si_{0.75}Ge_{0.25}$ was then performed on all wafers. Fig. 2(b) shows the cross-sectional profile of a fin (without SiN stringer) with SiGe S/D grown on the fin sidewalls, forming a Π-shaped SiGe S/D. Fig. 2(c) shows the *e*Π-SiGe S/D which extends into the buried oxide and encroaches under the Si fin (without SiN stringer) to give a more highly strained Si fin. S/D formation, oxide passivation, and metallization were performed to complete the devices. We shall compare the performances of FinFETs with Π-SiGe S/D [Fig. 2(b)] and *e*Π-SiGe S/D [Fig. 2(c)].

3. RESULTS AND DISCUSSION

Fig. 3 shows the results of a 3D stress simulation for a FinFET having *e*Π-SiGe S/D stressors. The recess in the BOX is 6 nm. A 2D cross-sectional view was taken close to the fin sidewalls so that SiGe regions of the *e*Π-SiGe stressor appear on the top and bottom of the Si fin in the S/D regions. The Si fin in the S/D region is under tensile stress (indicated by arrows in Fig. 3). This tensile stress in the S/D is larger in the device with *e*Π-SiGe S/D (Fig. 3 & 4). Consequently, the channel stress is more compressive for the FinFET with *e*Π-SiGe S/D stressors, as portrayed in Fig. 4. A TEM image of the gate stack (Fig. 5) shows a gate length L_g of 67 nm. For the *e*Π-SiGe structure, the recess in the BOX is clearly seen. This recess allows the growth of SiGe below the base of the Si fin (Fig. 6, bottom). This is not observed for the Π-SiGe structure where the BOX is not recessed (Fig. 6, right). The additional SiGe growth enhances the channel strain contribution from the SiGe S/D stressors.

FinFETs with 2 orientations (Fig. 7) are examined: θ = 0° and 45°, having strong and weak piezoresistance coefficients, respectively. Fig. 8 plots the I_{off}-I_{on} data for <100>-oriented (θ = 45°) FinFETs with Π-SiGe and *e*Π-SiGe S/D, showing little difference due to the negligible piezoresistance effect for that orientation. Fig. 9 reveals that if the channel orientation is <110> (θ = 0°), FinFETs with *e*Π-SiGe S/D give a 21% larger I_{on} at an I_{off} of 100 nA/μm over FinFETs with Π-SiGe S/D. Devices in Fig. 8 & 9 have W_{fin} = 100 nm. Fig. 10 shows the I_D-V_G characteristics of two closely matched FinFETs having W_{fin} = 60 nm, with similar series resistance, subthreshold swing and DIBL. Fig. 11 compares their I_D-V_D characteristics, showing the significant I_{on} enhancement achieved/contributed by the *e*Π-SiGe S/D stressor over a Π-SiGe S/D. This enhancement is largely attributed to the increase in hole mobility as suggested by the transconductance G_m gain in Fig. 12. A significant 71% increase in the peak G_m value is observed. Fig. 13 shows the I_{off}-I_{on} plots for FinFET with Π- and *e*Π- SiGe S/D stressors having W_{fin} = 60 nm. When W_{fin} is reduced from 100 to 60 nm, a significantly larger enhancement in I_{on} (50%) can be observed due to a larger strain effect and also a larger I_{on} contribution by the sidewalls which benefits more from the *e*Π-SiGe S/D. Fig. 14 and 15 show the enhancement in both $I_{D,Lin}$ and $I_{D,Sat}$ for FinFETs with *e*Π-SiGe S/D over FinFETs with Π-SiGe S/D. The enhancement in $I_{D,Lin}$ (~75%) is about 2× higher than that of I_{Dsat} or I_{on} (33%) for a given DIBL.

4. CONCLUSION

P-channel FinFETs with *e*Π-SiGe S/D stressors were demonstrated for the first time, showing a further I_{on} enhancement of up to 33% over FinFETs already strained by Π–shaped SiGe S/D stressors. I_{on} enhancement increases with reduced fin width. *e*Π-SiGe S/D stressors offer the highest compressive strain for hole mobility enhancement among the SiGe S/D stressor configurations explored to-date. This is made possible by a recessed buried oxide prior to selective epi-growth of SiGe. The integration scheme for *e*Π-SiGe S/D is very attractive as no additional process complexity is introduced. The *e*Π-SiGe S/D is promising for performance enhancement in aggressively scaled FinFET devices.

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REFERENCES

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[2] T.-Y. Liow *et al.*, *Symp. VLSI Tech. 2006,* pp. 68-69.
[3] P. Verheyen *et.al.*, *Symp. VLSI Tech. 2005*, pp. 194-195.

- Fin definition
- Gate Stack formation and Gate implant
- SDE implantation
- Spacer formation
- Removal of Spacer Stringer
- ***Pre-Epi HF Dip:***
  - ***Π SiGe S/D stressor : 30 sec***
  - ***eΠ SiGe S/D stressor: 120sec***
- $Si_{0.75}Ge_{0.25}$-Epi Growth
- S/D Implantation and Activation
- Metallization

Fig. 1. Process flow for the fabrication of FinFETs with *e*Π SiGe S/D stressor formed by introducing a longer pre-epi HF clean.

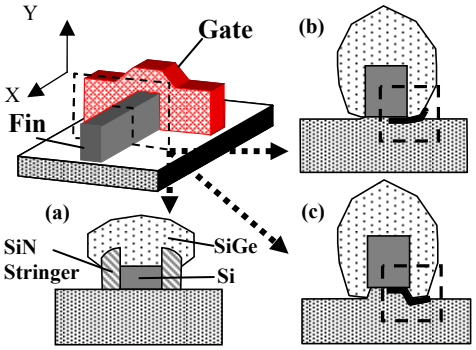

Fig. 2. (a) SiGe S/D stressor from ref 3. This work realizes (b) Π-SiGe S/D stressor. (c) *e*Π-SiGe S/D stressor with SiGe growth below the BOX.

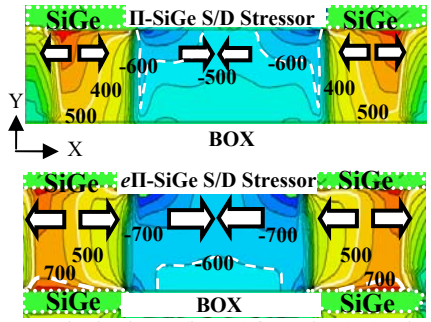

Fig. 3. Simulated stress (in MPa) for Π-SiGe (top) and *e*Π-SiGe S/D stressor (bottom) stressors. Contour interval is 100MPa. L_g = 40 nm, W_{fin} = 20 nm. Si at S/D and channel region is under tensile and compressive strain respectively.

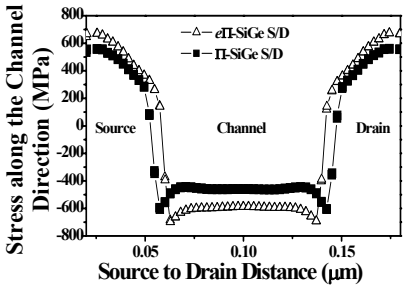

Fig. 4. Simulated stress along the channel direction taken near the bottom of the fin. *e*Π-SiGe S/D stressor has a larger tensile stress near to the BOX at the S/D region which result in a higher compressive stress in the channel.

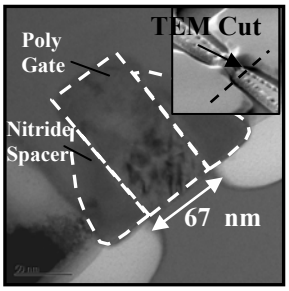

Fig. 5. TEM image of the gate profile taken along the S/D direction shows a gate length of sub 67nm. SEM image in the inset shows the FinFET having a raised SiGe S/D.

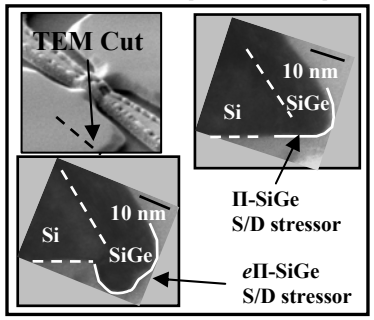

Fig. 6. TEM images taken at the edge of the FinFET device near the S/D region. SiGe is observed to have grown below the bottom of the fin for the *e*Π-SiGe S/D device.

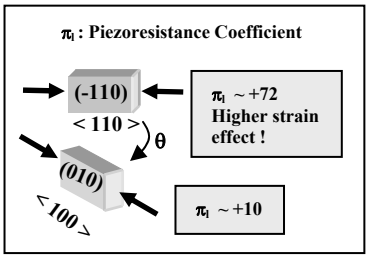

Fig. 7. Schematic showing the fin sidewall surface orientation and transport direction with the respective longitudinal piezoresistance coefficient.

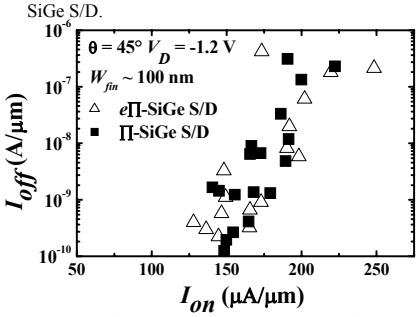

Fig. 8. I_{off} (V_G = 0.15 V) - I_{on} (V_G = -1.05 V) comparison showing not much difference between *e*Π and Π-SiGe S/D stressors for FinFETs having the <100> channel direction.

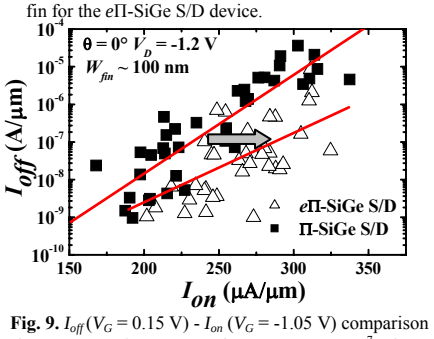

Fig. 9. I_{off} (V_G = 0.15 V) - I_{on} (V_G = -1.05 V) comparison shows an I_{on} enhancement of 21% at I_{off} = 1×10^{-7} A/μm for FinFET having *e*Π-SiGe S/D stressor over Π-SiGe S/D stressor. Channel direction is <110>.

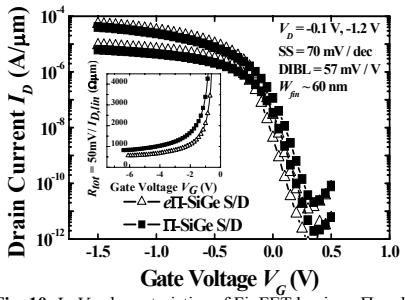

Fig. 10. I_D-V_G characteristics of FinFET having *e*Π and Π-SiGe S/D stressors shows similar subthreshold swing and DIBL value. Inset shows that both devices have matched S/D resistance.

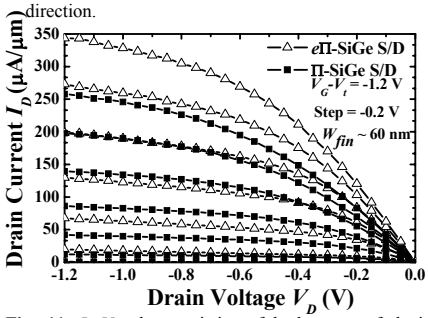

Fig. 11. I_D-V_D characteristics of both types of devices showing a higher drive current for FinFET having *e*Π-SiGe S/D stressors.

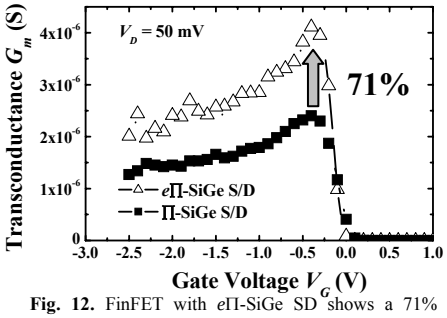

Fig. 12. FinFET with *e*Π-SiGe SD shows a 71% transconductance enhancement.

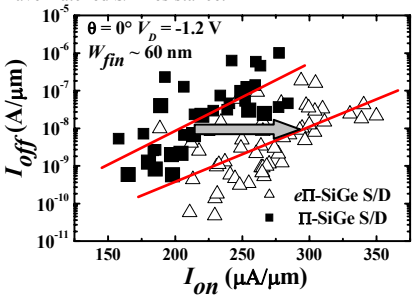

Fig. 13. I_{off} (V_G = 0.15 V) versus I_{on} (V_G = -1.05 V), showing larger enhancement [~50% at I_{off} = 1×10^{-8} (A/μm)] for W_{fin} of 60 nm over 100 nm.

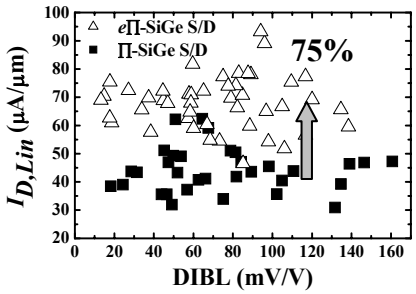

Fig. 14. $I_{D,Lin}$ obtained at V_G-V_t = -1.2 V and V_D = -0.1 V. 75% enhancement in linear drain current is observed for a given DIBL.

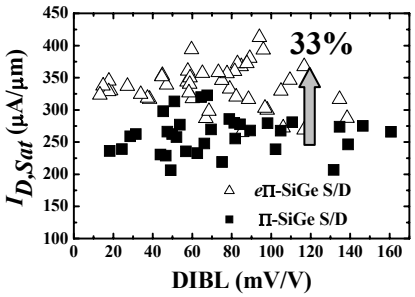

Fig. 15. $I_{D,Sat}$ obtained at V_G - V_t = V_D = -1.2 V. 33% enhancement in drive current can be observed at a fixed DIBL.