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Impact of Gradual Source/Drain Impurity Profiles on Performance of Germanium Channel Double-Gated pMISFETs

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1. Introduction

Germanium is an attractive material to improve on-state current (I_{ON}) for future advanced MISFETs due to its high mobility, although there is a concern about off-state current (I_{OFF}) increase caused by the small band-gap. Diffusion and generation-recombination currents in Ge have been reported to be sufficiently low for the requirement of low standby power operation [1]. However, I_{OFF} due to band-to-band tunneling can be still a critical issue. Detailed simulation results of I_{OFF} due to direct and indirect tunneling in many-valley band structure and I_{ON} based on non-equilibrium Green's Function or Monte Carlo approaches have been reported [2,3]. The previous papers have mainly discussed I_{ON} improvement for devices with abrupt S/D in high I_{OFF} (0.1μA/μm) region. However, a benefit of Ge-MISFETs under low I_{OFF} condition, which is important for practical SoC application, has not been clarified yet. On the other hand, gradual and offset source/drain (S/D) profiles are known to be effective in reducing I_{OFF} of Si-MISFETs with minimizing I_{ON} degradation due to parasitic resistance [4]. In this paper, thus, I_{ON}-I_{OFF} characteristics of ultra-thin body Ge channel double-gated pMISFETs (DG-pMISFETs) having various gradual S/D profiles are quantitatively examined.

2. Simulation

P-channel DG-MISFETs shown in Fig. 1 were investigated by a drift-diffusion device simulator. S/D profile was represented by the Gaussian distribution. Mobility of Ge was adjusted to be 3 times higher than that of Si on a basis of the experimental result [5]. Saturation velocity was adjusted to be 1.7 (= $(\mu_{Ge}/\mu_{Si})^{1/2}$) times higher with considerations on the non-steady transport in sub-100 nm gate length [6]. Band-to-band tunneling was calculated by WKB approximation using band-gap and tunnel mass (0.17 m_0 for Si and 0.063 m_0 for Ge). Fig. 2 shows typical I_D-V_G characteristics. We defined I_{OFF} as I_D at the minimum value. I_{ON} was defined as I_D at $V_G = V_D - V_{OFF}$, where V_{OFF} was V_G at I_{OFF}. V_{OFF} can be shifted to 0V by adjusting gate workfunction. Fig. 2 also shows that I_{OFF} of Ge-MISFETs is about 10^4 times higher than that of Si-MISFETs due to lower band-gap. In case of ultra-thin body less than 10nm, band-gap widening due to quantum confinement shown in Fig. 3 was taken into account. Fig. 4 shows the body thickness dependence of I_{OFF}. I_{OFF} in this work almost agrees with calculations using a precise model [3].

3. Concept of Gradual S/D Structure

For reducing I_{OFF}, the high electric field at drain edge should be lowered. There are several ways to reduce I_{OFF} such as V_D reduction, offset S/D profile (δ increase) and gradual S/D profile (σ increase). Fig. 5 shows I_D-V_G characteristics with various δ. The 3 orders of magnitude of I_{OFF} reduction is obtained at δ=20nm. However, severe I_{ON} degradation is also induced. Fig. 6 shows the V_D, δ and σ dependence of I_{ON}-I_{OFF} characteristics. Reduction of V_D leads to the worse I_{ON} degradation due to gate overdrive reduction. Gradual S/D profile with adequate σ (σ=7nm in case of δ=25nm) gives optimum I_{ON}. Fig. 7 shows impurity profile at (I_{ON}, I_{OFF}) point indicated as *1*, *2*, *3* and *a* in Fig. 6. When σ is small (point 1), parasitic resistance decreases I_{ON}. On the other hand, when σ is large (point 3), I_{ON} degradation is caused by short channel effects. Therefore, spread I_{ON}-I_{OFF} characteristics are obtained by varying δ and σ, and the right edge of I_{ON}-I_{OFF} characteristics gives optimum I_{ON}.

4. I_{ON}-I_{OFF} Characteristics of Ge- and Si-DGMISFTEs

According to the gradual S/D concept discussed above, I_{ON}–I_{OFF} characteristics of Ge- and Si-DGMISFEs were compared in range of δ=0.1-30nm and σ=0.1-10nm. Fig. 8 shows the results for the body thickness T=10nm case. It is found that the I_{ON}-I_{OFF} curve of Ge intersects the I_{ON}-I_{OFF} curve of Si at critical I_{OFF} ($I_{OFF\ CRITICAL}$) of around 2nA/μm. Ge-MISFETs can yield higher I_{ON} in the region of $I_{OFF} > I_{OFF\ CRITICAL}$ than Si-MISFETs. Fig. 9 shows the I_D-V_G characteristics and the S/D profiles for Ge- and Si-MISFETs with I_{OFF}=5nA/nm. The smaller sub-threshold swing is obtained in Ge-MISFETs in spite of the higher dielectric constant of Ge, which can cause severe short channel effects. This is another advantage of the gradual S/D structure. As a result, 20% higher I_{ON} is obtained for Ge-MISFETs.

Fig. 10 shows I_{ON}–I_{OFF} characteristics when body thickness is reduced to 3nm. The I_{ON}-I_{OFF} curve for Ge-MISFETs shifts to lower I_{OFF} direction than the case with T=10nm, although both I_{ON}-I_{OFF} curves in Si-MISFETs with 3nm and 10nm are almost the same. Therefore, $I_{OFF\ CRITCAL}$ can be reduced down to sub-100pA/μm, which is the same order of the magnitude as that for low standby power operation. The body thickness dependence of critical I_{OFF} is shown in Fig. 11. Fig. 12 shows the I_D-V_G characteristics and the S/D profile for Ge- and Si-MISFETs with I_{OFF}<100pA/nm. More than 20% I_{ON} improvement is found to be still achieved.

5. Conclusion

In order to evaluate the performance of ultra-thin body Ge channel double-gated pMISFETs in low I_{OFF} (<0.1μA/μm) region, device characteristics with gradual S/D structures were simulated at L_G=20nm, EOT=1.2nm and V_D=-1V. When the body thickness is 10nm, 20% higher I_{ON} than that in Si is obtained at the same I_{OFF} of 5nA/μm. As the body thickness is further reduced to 3nm, 20% I_{ON} improvement is still achieved at I_{OFF}<100pA/μm. These results demonstrate that UTB Ge-channel DG-pMISFETs are also attractive for general purpose application, not only for high performance application.

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References

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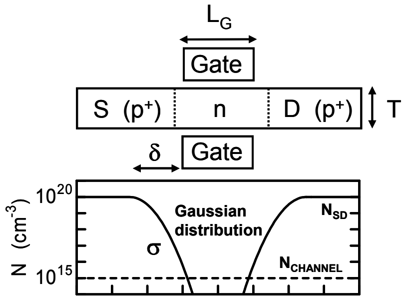

Fig. 1 Simulated device structure and impurity profile. Source/Drain profile is represented by a displacement Gaussian profile, where δ is offset length and σ is standard deviation.

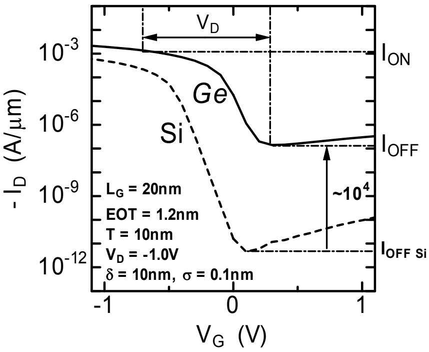

Fig. 2 I_D-V_D characteristics of Ge- and Si-DGMISFETs. Definition on I_{ON} and I_{OFF} in this paper is also shown.

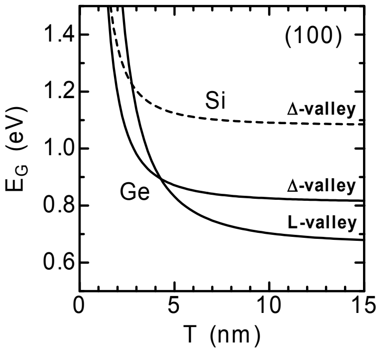

Fig. 3 Band-gap as a function of body thickness.

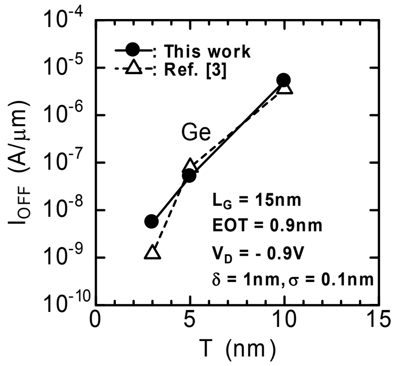

Fig. 4 Body thickness dependence of I_{OFF} for Ge-DGMISFETs with abrupt S/D profile. Note that device parameters are different from other figures for comparison.

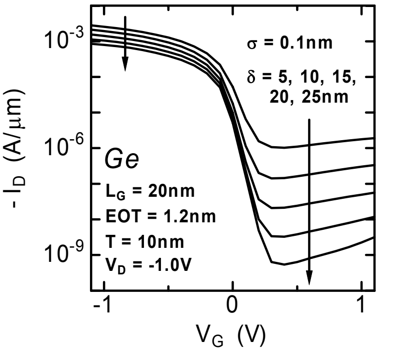

Fig. 5 I_D-V_G characteristics of Ge-DGMISFETs with abrupt S/D profiles and various offset length δ. I_{OFF} decreases as δ increases.

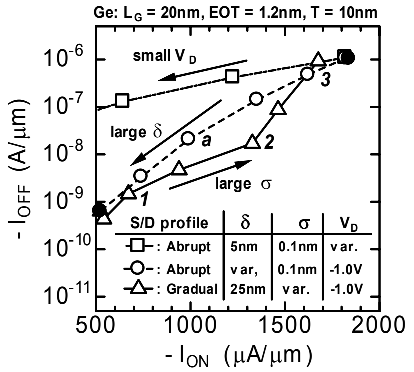

Fig. 6 I_{ON}-I_{OFF} characteristics of Ge-DGMISFETs with various drain voltage (V_D), offset length (δ) and standard deviation (σ). S/D profiles at (I_{ON}, I_{OFF}) points indicated by *1*, *2*, *3*, and *a* are shown in Fig. 7.

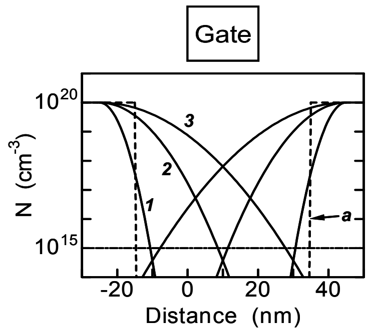

Fig. 7 S/D profiles corresponding to (I_{ON}, I_{OFF}) points indicated as *1*, *2*, *3* and *a* in Fig. 6. Profile 2 gives optimal I_{ON} at δ=25nm for Ge-DGMISFET.

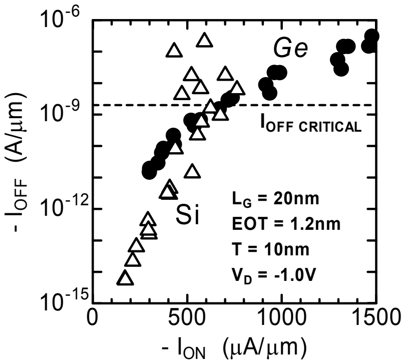

Fig. 8 I_{ON}-I_{OFF} characteristics of Ge- and Si-DGMISFETs with various S/D profiles. The body thickness T is 10nm.

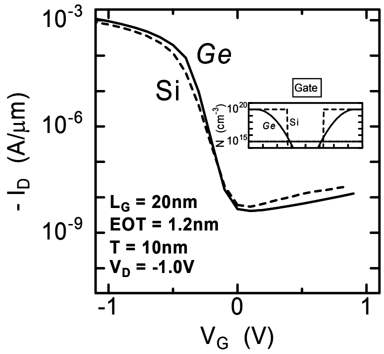

Fig. 9 I_D-V_G characteristics of Ge- and Si-DGMISFETs with I_{OFF} = 5nA/μm. The body thickness T is 10nm. I_{ON} of Ge is 20% higher than that of Si. The insertion is the impurity profile corresponding to the electrical characteristics.

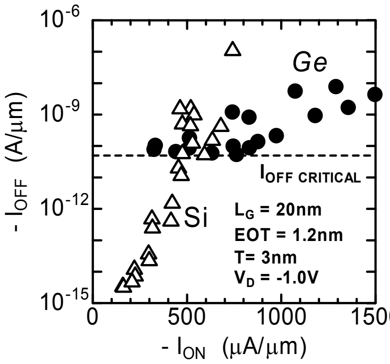

Fig. 10 I_{ON}-I_{OFF} characteristics of Ge- and Si-DGMISFETs with various S/D profiles. The body thickness T is 3nm.

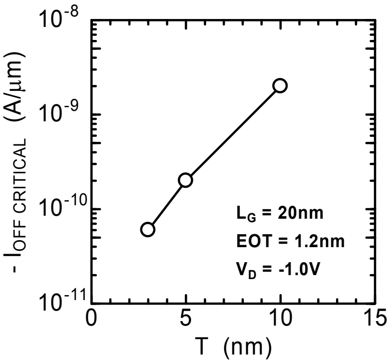

Fig. 11 Body thickness dependence of critical I_{OFF} considering gradual S/D profiles. Higher I_{ON} of Ge-DIMISFETs than that of Si-DGMIFETs is achieved for I_{OFF} > $I_{OFF\ CRTICAL}$.

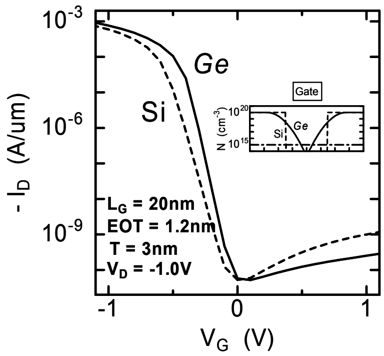

Fig. 12 I_D-V_G characteristics of Ge- and Si-DGMISFETs with I_{OFF} < 100pA/μm. The body thickness T is 3nm. I_{ON} of Ge is 20% higher than that of Si. The insertion is the impurity profile corresponding to the electrical characteristics.