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# A Double-Gate Tunneling Field-Effect Transistor with Silicon-Germanium Source for High-Performance, Low Standby Power, and Low Power Technology Applications

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## ABSTRACT

In this paper, we propose a novel Double-Gate (DG) Tunneling Field-Effect Transistor (TFET) with Silicon-Germanium (SiGe) Source to overcome the scaling limits of CMOS technology. For the first time, such a technology proves to be viable to replace CMOS for high performance, low standby power, and low power technologies through the end of the roadmap by optimizing the device parameters and Ge content in the source. Less than 60 *mV/decade* subthreshold swing with extremely low off-state leakage current is achieved for such a device. The narrower bandgap of SiGe results in a narrower tunneling width, hence improving the subthreshold swing and on-state current.

## INTRODUCTION

The Tunneling Field-Effect Transistors (TFET) has been proposed as an alternative device structure to curb the rapidly increasing power consumption in conventional CMOS circuits [1]. The TFET operation exploits the gate-controlled band-to-band tunneling mechanism to overcome the fundamental $kT/q$ thermodynamic limit placed on the abruptness of the subthreshold swing in conventional MOSFETs [2]. Due to the reverse biased p-i-n diode configuration, TFET exhibits excellent short channel effect (SCE) and extremely low off-state leakage $I_{off}$. However, single-gate TFET devices are limited in the amount of current they could conduct as band-to-band tunneling is a strong surface phenomenon. As such, its establishment as a future CMOS-compatible technology is seriously affected. In order to meet the requirement of the International Technology Roadmap for Semiconductor (ITRS) [3], further current enhancement is needed.

In this paper, a Double-Gate (DG) TFET structure [Fig. 1(a)] is proposed and extensively studied using TCAD tools to explore its scalability and suitability for high performance (HP), low power (LP), and low standby power (LSTP) technology. With the additional gate giving rise to gate-to-gate coupling effects, the current more than doubles with optimal silicon film thickness.

## DEVICE STRUCTURE AND MODELING

The basic device structure of the DG TFET is shown in Fig. 1(a). A $Si_{1-x}Ge_x$ source is incorporated in Fig. 1(b) for performance enhancement. With the help of Synopsys TCAD tools [4], the band-to-band tunneling rate is modeled using Kane's model [5] as follows.

$$G_{BTBT} = A\xi^2 E_g^{-1/2} \cdot \exp\left(-B\frac{E_g^{3/2}}{\xi}\right), \quad (1)$$

where $\xi$ and $E_g$ are the electric field and bandgap respectively. $A$ and $B$ are functions of carrier effective mass and the tunneling barrier width $\omega_T$ (Fig. 4). For all simulations, a high-k gate dielectric ($HfO_2$) is employed. Gaussian doping with peak concentration of $10^{20}$ $cm^{-3}$ and $10^{19}$ $cm^{-3}$ is assumed for the source and drain doping respectively. The channel has a p-type concentration of $5x10^{16}$ $cm^{-3}$.

## RESULTS AND DISCUSSION

### A. Device Characteristics

For device operation, the source is grounded with the drain at a positive bias. In the off-state, the gate bias is zero and there is insufficient band bending for tunneling to occur. As such, the leakage current of the device will be extremely low. In the on-state, the gate induces sufficient band bending such that the tunneling barrier width $\omega_T$ narrows to below 5nm. Hence, band-to-band tunneling of electrons from the valence band of $p^+$ source to the conduction band of $n^+$ drain could occur readily. Due to the exponential relationship between band-to-band generation rate and electric field, the subthreshold swing of the TFET device could be lower than the theoretical limit of 60 *mV/decade* in conventional MOSFETs at room temperature.

Fig. 2 plots the gate transfer characteristics of n-channel and p-channel DG TFET devices with $Si_{0.8}Ge_{0.2}$ source. Excellent subthreshold swing is achieved with high $I_{on}$-$I_{off}$ ratio. Incorporating germanium into silicon reduces the bandgap $E_g$, and hence the tunneling width $\omega_T$ [Fig. 3]. This is illustrated by the energy band diagram in Fig. 4. Electrons are able to tunnel more easily through the narrower $\omega_T$, leading to a significant increase in band-to-band tunneling rate $G_{BTBT}$ [Fig. 5]. As such, the gate transfer characteristic of DG TFET improved with increasing Ge content [Fig. 6]. Higher $I_{on}$ is achieved with improved subthreshold swing. The subthreshold swing $S$ improves as the Ge content increases [Fig. 7]. Due to the narrower $\omega_T$, the threshold voltage $V_T$ also decreases. Fig. 8 shows how the $V_T$ changes as a function of Ge content for two different power supply $V_{DD}$ requirements. In order to meet the ITRS roadmap requirement, $I_{on}$ and $I_{off}$ could be tuned using different Ge content for different technology requirements [Fig. 9 and Fig. 10]. In general, both $I_{on}$ and $I_{off}$ increases as Ge content increases.

### B. Roadmap Benchmarking

Fig. 11 depicts the $V_{DD}$ requirements at each technology node [3]. Due to the better $I_{on}/I_{off}$ tradeoff in DG TFET, the dynamic power consumption can be decreased in LSTP devices by using lower $V_{DD}$. To investigate this possibility we perform device optimization for LSTP devices using HP Vdd requirements (LSTP: HP $V_{DD}$). DG TFET devices are optimized and the Ge content required at each technology nodes for different technology is shown in Fig. 12. In general, as $I_{on}$ requirement increases for various technologies, the Ge content required also increases. For LSTP technology, the $V_{DD}$ and $I_{on}$ requirements are not so stringent. Hence, the Ge content required is much lower. For HP and LP technologies, higher Ge content is needed for a better subthreshold swing and a higher $I_{on}$-$I_{off}$ ratio. The resulting $V_T$ for each technology node is shown in Fig. 13.

Fig. 14 depicts the $I_{off}$-$I_{on}$ plot for HP and LP technology nodes using DG TFET with SiGe source. The $I_{off}$, and hence the static power consumption is at least a few orders lower than the ITRS requirements. However, at the end of the roadmap, higher Ge content is used and the $I_{off}$ increases rapidly. However, it still remains much lower than the requirement. The resulting $I_{on}$, and thus the driving frequency is also much higher at each technology node. In fact, higher $I_{on}$ could be achieved by trading off $I_{off}$, which is far below the specification. Fig. 15 shows the roadmap requirements for LSTP and DG TFET LSTP (LSTP: HP $V_{DD}$) devices at each technology node. It is noted here that two different $V_{DD}$'s are used. The lower $V_{DD}$ allows the realization of lower dynamic power consumption (up to 36% dynamic energy savings at LSTP22) for the low standby power devices. Nevertheless, all requirements are met with extremely low power consumption. Hence, DG TFET technology proves to be a viable technology to replace the conventional CMOS technology, satisfying HP, LP, and LSTP specifications.

## CONCLUSION

A DG TFET technology was studied and explored through detailed TCAD simulation. The use of narrower bandgap material like SiGe in the source has enhanced the band-to-band generation rates, subthreshold swing and on-state current. The low leakage current in the DG TFET also gives rise to low power consumption. By optimizing the devices and benchmarking against the ITRS roadmap, DG TFET technology proves to be scalable, and is a viable technology to replace/co-integrate with the CMOS technology, for high performance, low power, and low standby power logic applications.

## REFERENCES

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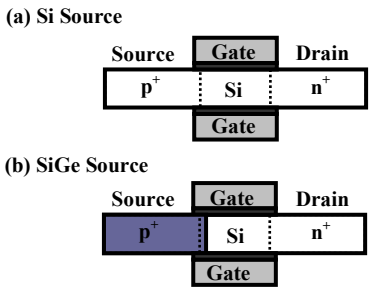


**Fig. 1**. Schematic of (a) DG TFET transistor, (b) DG TFET transistor with SiGe source. For an nFET, the drain is doped $n^+$ while source is doped $p^+$.

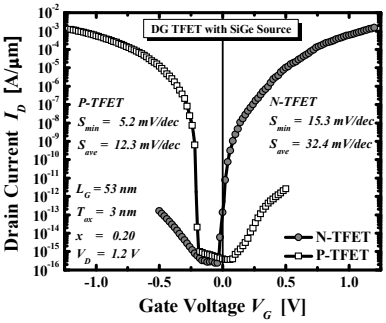


**Fig. 2**. Gate transfer characteristics of DG CTFET with $Si_{0.8}Ge_{0.2}$ Source show Excellent subthreshold swing is achieved.

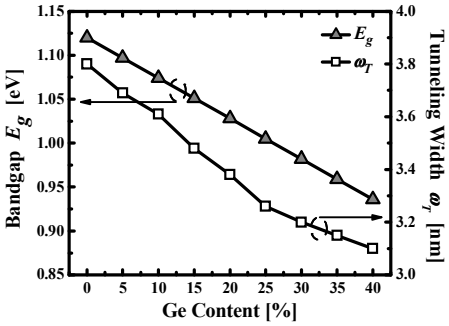


**Fig. 3.** With increasing Ge content, bandgap $E_g$ and tunneling width $\omega_T$ decreases,and tunneling is enhanced.

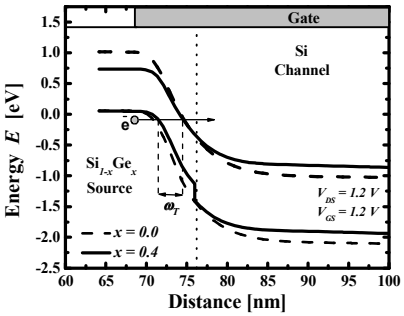


**Fig. 4.** Energy Band Diagram of DG TFET with $Si_{1-x}Ge_x$ source where $x = 0$, and $x = 0.4$. Higher Ge content reduces the tunneling width $\omega_T$ substantially.

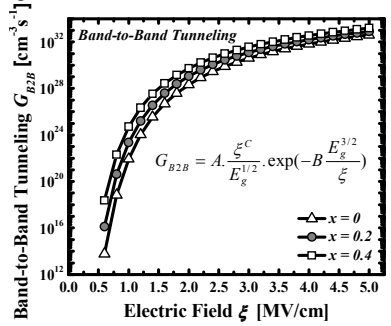


**Fig. 5.** Band-to-band tunneling (BTBT) rate increases as the Ge content increases. Higher BTBT rate is favorable for TFET operation.

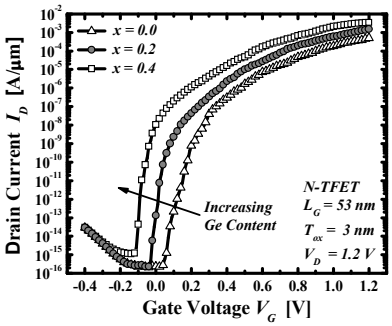


**Fig. 6.** Plot of simulated $I_D$-$V_G$ for DG TFET with SiGe source. Increasing Ge content enhances the drive current and the subthreshold swing.

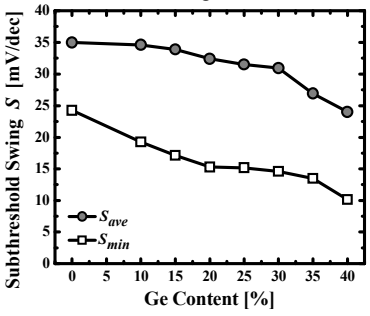


**Fig. 7.** The subthreshold swing improves as the Ge content is increased.

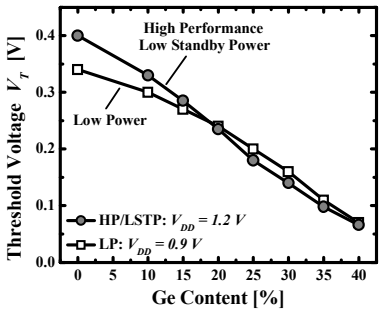


**Fig. 8.** Threshold voltage reduces with increasing Ge content and can be tuned to a desired value .

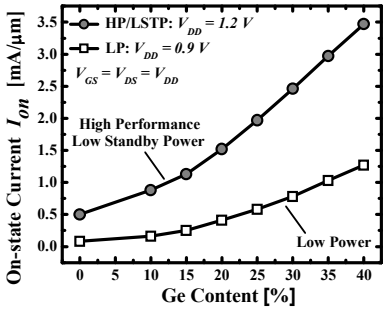


**Fig. 9.** BTBT rate and hence $I_{on}$ is enhanced with the incorporation of higher Ge content.

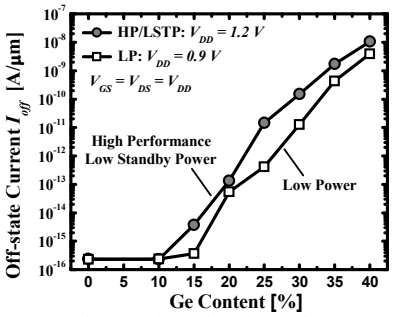


**Fig. 10.** The $\omega_T$ is reduced as the Ge content increases, hence giving rise to increasing $I_{off}$. Higher $V_{DD}$ also results in higher $I_{off}$ (reducing $\omega_T$).

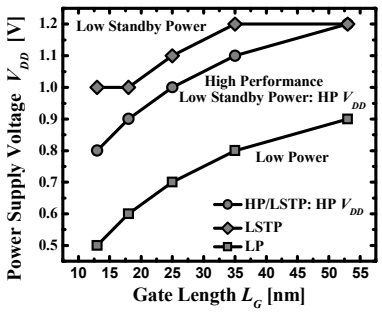


**Fig. 11.** Power Supply voltage scaling for various technology nodes. LSTP:HP $V_{DD}$ logic uses a lower $V_{DD}$ than LSTP logic to reduce dynamic power.

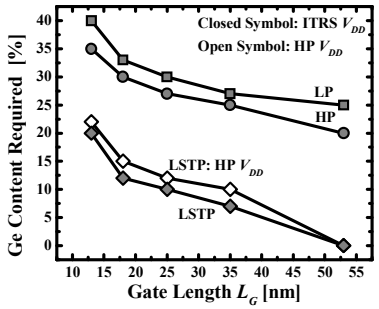


**Fig. 12.** Higher Ge content is required at shorter $L_G$, and for LP and HP logic devices due to more stringent performance requirements.

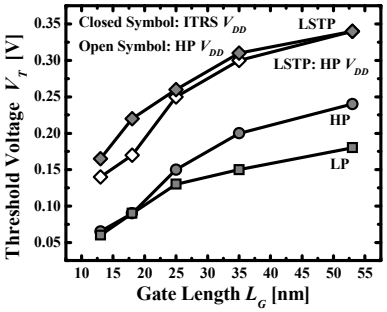


**Fig. 13.** The threshold voltages using DG TFET for various technologies could be much lower than that specified by ITRS roadmap due to good $S$ and $I_{off}/I_{on}$.

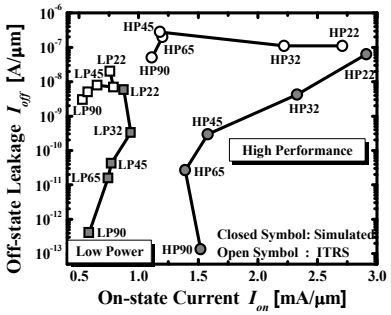


**Fig. 14.** High Performance (HP) and Low Power (LP) logic devices using DG TFET perform impressively when benchmarked against ITRS.

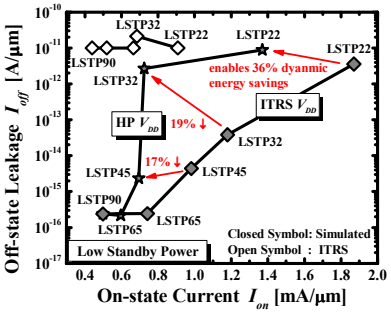


**Fig. 15.** Using a lower $V_{DD}$ (LSTP:HP $V_{DD}$) helps to reduce dynamic power and allows for possible integration with HP logic using a common $V_{DD}$.