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Electrical properties of carbon nanotubes grown at a low temperature by radical chemical vapor deposition for future LSI interconnects

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1. Introduction

Carbon nanotube (CNT) is one of promising materials for future LSI interconnects because of its unique properties such as high current density exceeding 10^9 A/cm^2, high thermal conductivity and ballistic transport. For interconnect application, it is essential to synthesize densely-packed CNT-bundles at a low temperature below 400˚C [1]. Although a few groups reported CNTs via process [2-5], there is no report about electrical properties of CNTs grown under 400˚C. In this study, we report the electrical properties of CNTs grown in via-holes at 390˚C by radical CVD [6]. In addition, we succeeded in improving the resistivity of CNT-via by 400˚C annealing in the hydrogen atmosphere.

2. Experimental

We fabricated CNT vias shown in Figure 1. Bottom electrodes are composed of Cu wiring (100 nm) covered by Ta barrier layer (15 nm). TiN contact and buffered layer (5 nm) was sputtered on the bottom electrodes. After depositing a tetraethylorthosilicate (TEOS) dielectric layer (250 nm), via holes were made using conventional photolithography and buffered hydrofluoric (BHF) wet etching. The size of via holes ranges from 2 to 10 μm. The Co catalyst particles for CNT growth were size-classified using impactor [5] and were deposited on TiN layer with the average diameter of 3.8 nm. The size-classified catalyst particles deposited directly on buffered layer can be denser than particles formed by heating films because the diameter of latter have broad distribution and such particles can't realize close-packed.

For CNTs growth, we used the radical CVD equipment with an antenna and the spherical plasma is generated by microwave (2.45 GHz) at the edge of the antenna [6]. The source gas for CNT growth was a mixture of H_2 and CH_4 at 20 Torr and the microwave power was 60 W. Although our method uses plasma, there is little damage to sample on the substrate because the plasma is fixed to the antenna edge and the substrate holder is located 50 mm away from the discharging area. When we grounded the antenna and applied negative bias voltage to the substrate, no distinct current was measured. Therefore, there are no positive ions, which affect the CNTs growth, around the substrate and only radicals contribute to CNTs growth. Furthermore, the growth temperature depends on only the heater, which indicates that our equipment is suitable for low temperature growth of CNTs. The growth temperature of CNT-bundles was 390˚C under the allowing temperature of 400˚C in Si LSI process.

To measure electrical properties, Ti contact layer (10 nm) and Cu wiring (300 nm) were sputtered as the top electrodes on CNTs. Cu wiring is covered by Ta barrier layer (15 nm) to protect from oxidation. Via resistances were measured with a four-point probe method at room temperature. After measuring electrical properties of CNTs, the CNT vias were annealed at 400˚C for 30 min in the hydrogen atmosphere. We evaluated the change of resistivity of CNT-vias by annealing.

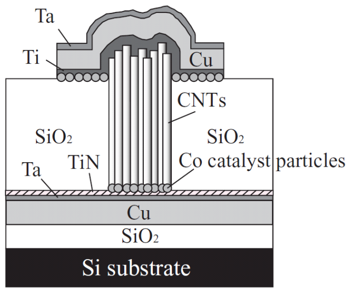

Fig. 1 The structure of CNT via for electrical properties

3. Result and Discussion

Figure 2 shows (a, b) SEM and (c) TEM images of vertically aligned CNTs grown at 390˚C for 30 min in 2-μm-diameter via-holes. CNTs grow equally in all holes with good reproducibility. The diameter of grown CNTs ranges 5 to 10 nm (avg. 7 nm) and the density of CNT is 1.6×10^{11} cm^{-2} which corresponds to one-tenth of the close-packed density of 7 nm CNT. As shown in Figure 3 (b), vertically aligned CNTs grow densely. The TEM image shown in Fig. 2 (c) indicates that a CNT grown at the low temperature of 390˚C maintains a hollow structure, having a good quality of graphite sheets enough to realize the carrier conduction. The main path for carrier conduction is outermost graphite sheets of CNT because the top of CNT is capped and electrodes only make contact with surface of CNTs. Figure 3 (a) shows that vertically aligned CNTs selectively grow from via-holes and CNTs don't grow from Co catalyst particles on the SiO_2 dielectric layer. We think that the interface reaction between Co particles and TiN buffered layer plays an important role for CNT growth.

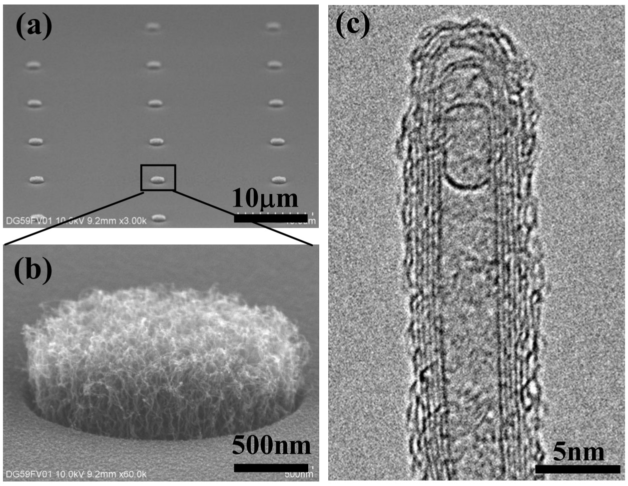

Fig.2 (a), (b) SEM images and (c) high magnification TEM image of CNT grown at 390˚C in via holes

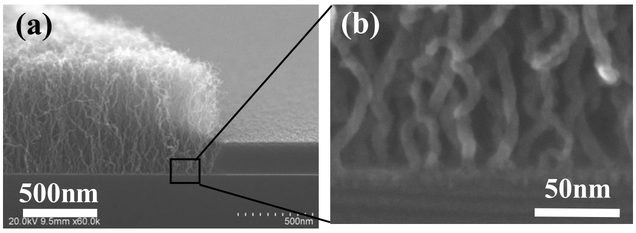

Fig. 3 (a) Cross-sectional and (b) high resolution SEM images of CNTs grown in square via holes

Figure 4 (a) shows ohmic behaviour between CNTs and electrodes before annealing. However, Figure 4 (b) shows that the resistance of CNT via is inversely proportional not to the via area but to the via diameter. The electrical contact is dominantly achieved at the surrounding of via. The measured via resistance of 36 Ω is lower than the calculated resistance of 79 Ω for outermost CNTs of CNT-via using quantum resistance (6.45 kΩ/tube). It indicates that the ohmic contacts are formed on the outermost of CNTs and slightly inner CNTs in the via area. However, most of inner CNTs may not be contributed to carrier conduction.

Figure 5 (a) shows that good ohmic behaviour is maintained and the 2-μm-diameter-via resistance decreased from 36 Ω to 16 Ω after 400˚C annealing. Although the improved via resistance of 16 Ω is still higher than the calculated resistance of ~1 Ω for all CNTs in the via expected from quantum resistance, the difference between them can be reduced. The ratio of CNTs which achieve ohmic contacs in the via hole is increased by annealing and total via resistance is improved. Figure 5 (b) shows that almost all via resistances are reduced after 400˚C annealing in the hydrogen environment. The effect of 400˚C annealing mainly contributed to the contacts between CNTs and top electrodes because bottom electrodes and CNTs were still heated at 390˚C when CNTs grew from via-holes. Although the resistivity of CNTs improved by annealing, they are still higher than that of metal via. The resistance is expected to be lowered further by improving not only the CNT density but also the electrical contact between inner CNTs and electrodes. Furthermore, the resistance is improved by opening the cap of CNT using chemical mechanical polishing (CMP) because the carrier path will increase by using inner graphite sheets of CNTs.

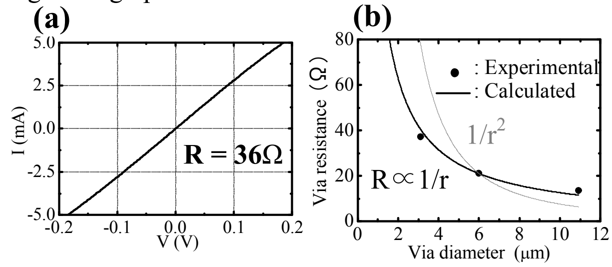

Fig.4 Electrical properties of CNT vias before annealing
(a) Current-voltage characteristics of 2-um-diameter CNT vias
(b) The relation between the via resistance and the via diameter

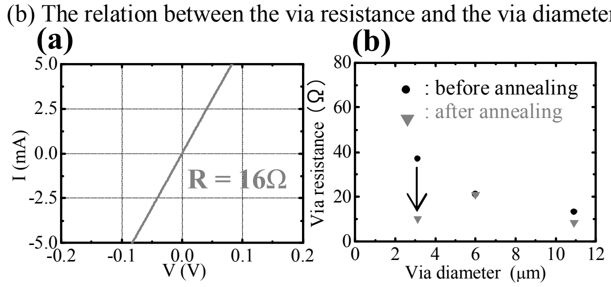

Fig. 5 Electrical properties of CNT vias after 400˚C annealing for 30 min in the hydrogen atmosphere
(a) Current-voltage characteristics of 2-um-diameter CNT vias
(b) The relation between the via resistance and the via diameter

4. Conclusion

We fabricated CNT-via grown at a low temperature of 390˚C using radical CVD and succeeded in measuring electrical properties of CNTs by achieving ohmic contacts. The resistance decreased after annealing at 400˚C in the hydrogen environment. Our growth method is expected to be useful for future multi-layer interconnects of LSI because thermal damage to LSI can be reduced.

Acknowledgements

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