Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 58-59

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Carbon Nanotube Vias Fabricated by Remote Plasma-Enhanced Chemical Vapor Deposition

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1. Introduction

Formation of reliable interconnects is one of the most important issues in fabricating ultra-large-scale integration (ULSI) devices.

Carbon nanotubes (CNTs) are a promising material for future ULSI interconnects due to their excellent properties such as high current capability, high thermal conductivity, ballistic transport along the tube and high aspect ratio. Recently, via interconnects using vertically aligned CNT bundles fabricated by chemical vapor deposition (CVD) have been intensively investigated [1-3]. It is necessary to lower the growth temperature of CNTs below 400 °C for the integration with low-dielectric-constant films in ULSI. Plasma-enhanced CVD is a suitable means to lower growth temperature of CNTs because source gases in the CVD can be decomposed even at low temperatures owing to plasma.

In this paper, we report on the low-temperature fabrication of CNT vias by remote plasma-enhanced CVD and their electrical properties.

2. Experimental

The growth of CNTs is performed using a surface-wave-excited microwave plasma-enhanced CVD system. A 2.54 GHz microwave is introduced into the vacuum chamber through a slot antenna and a quartz window. The plasma is generated near the surface of the quartz window. The distance between the plasma and the substrate was about 50 mm. A quarts ion trap and a metal mesh grid were installed between the plasma and the substrate stage for suppression of ion bombardment damage. We confirmed the effects on the reduction of ion density near the substrate by a Langmuir probe. The source gas was CH_4 diluted with H_2. The flow rates of CH_4 and H_2 were 10 and 90 sccm, respectively. The gas pressure and the microwave power were 10 Torr and 500 W. The substrate temperature was controlled with a graphite heater.

Formation of a planarized CNT via structure is performed using conventional semiconductor processes [1]. The substrate consisting of TiN/Ta/Cu layers was fabricated on 3-inch Si wafer. A SiO_2 dielectric layer was deposited by CVD using tetraethylorthosilicate (TEOS). Via holes with various diameters ranging from 1 to 10 μm were formed using conventional photolithography and wet etching. Size-classified Co nanoparticles generated by laser ablation and an impactor were deposited on the TiN surface [4]. In the via formation, CNT bundles were selectively grown in via holes at 430 °C. After the growth, chemical mechanical polishing (CMP) was applied for planarization of CNT vias. Finally, the upper electrodes composed of a Ti contact layer and a Cu wiring layer were formed. A schematic diagram of a planarized CNT via is shown in Fig. 1.

The resistance of CNT via was measured using a four-terminal Kelvin structure at room temperature.

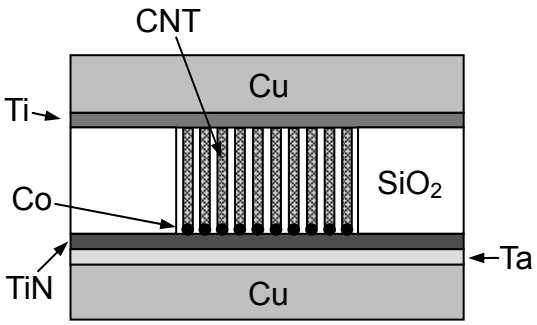

Fig. 1 Schematic diagram of planarized CNT via.

3. Results and Discussion

Figure 2 shows a transmission electron microscope (TEM) image of a CNT grown by remote plasma-enhanced CVD at 430 °C. A hollow structure in the center of the nanotube and a multi-walled structure of the CNT were observed. The diameter of the CNT was approximately 10 nm.

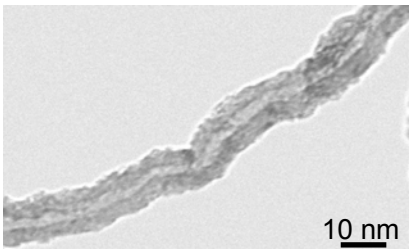

Fig. 2 TEM image of CNT grown by remote plasma-enhanced CVD at 430 °C.

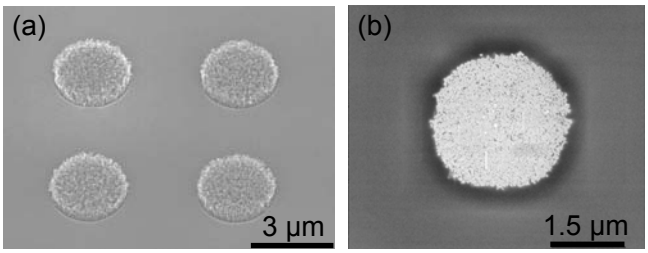

Fig. 3 SEM images of (a) multi-walled CNT bundles grown in via holes and (b) planarized CNT via after CMP.

Figures 3 (a) and (b) show scanning electron microscope (SEM) images of multi-walled CNT bundles grown in via holes by remote plasma-enhanced CVD at 430 °C. Vertically aligned CNT bundles were selectively grown on the bottom of via holes. The density of CNTs was estimated to be approximately 1×10^{11} cm^{-2}, which was ten times lower than the density of Co nanoparticles deposited on the bottom of a via hole. As shown in Fig. 3 (b), planarization of the CNT via was achieved by CMP.

Figure 4 shows typical current-voltage characteristics of planarized CNT vias of 1, 2, 5 and 10 μm in diameter. The resistances of the CNT vias were 180 Ω for 1 μm, 72 Ω for 2 μm, 16 Ω for 5 μm and 5 Ω for 10 μm, respectively. As for a 2-μm-diameter CNT via fabricated by thermal CVD at 510 °C, the resistance of 0.59 Ω has been reported [4]. The higher resistance obtained in the present study may be attributable to ion bombardment damage from plasma to CNTs. Further improvement of electrical properties of CNT vias is required. In order to lower the electrical resistance of a CNT via, it is important to grow high-quality dense CNTs.

The dependence of the via resistance on the via area is shown in Fig. 5.

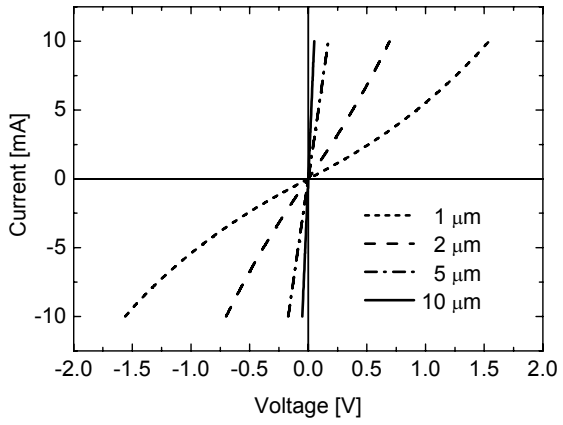

Fig. 4 Typical current-voltage characteristics of planarized CNT vias with various diameters.

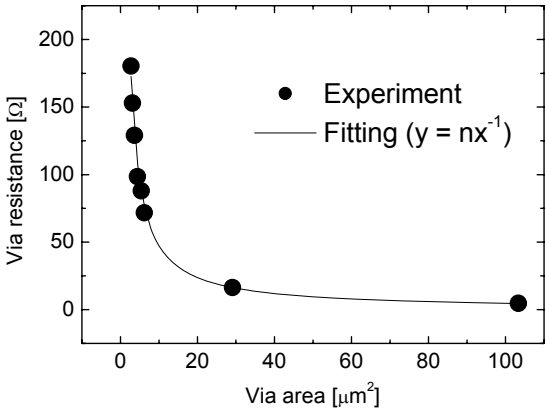

Fig. 5 Via resistance as a function of via area. A solid curve indicates the theoretical calculation.

Notice that the via resistance is in inverse proportion to the via area. This result indicates that the CNTs are grown with uniform quality and density in via holes with various diameters and good electrical contacts between CNTs and the electrodes are obtained.

4. Conclusion

We have succeeded in fabricating CNT vias at a low temperature of 430 °C using remote plasma-enhanced CVD, which is a promising method to lower the growth temperature of CNTs. Low-temperature growth of CNTs has been achieved owing to the reduction of ion density in plasma. We demonstrate the electrical properties of the planarized CNT vias with various diameters. The resistance of the CNT via is inversely proportional to the via area, which indicates good uniformity of the CNT growth and contact formation. We believe that remote plasma-enhanced CVD enable us to achieve lower temperature growth of CNTs with higher quality.

Acknowledgement

This work was performed as part of the MIRAI Project supported by NEDO.

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