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# A Novel Contact-plug Process with Low Resistance Nucleation Layer Using $B_2H_6$-reduction W-ALD Method for 32nm CMOS Devices and Beyond

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## 1. Introduction

With a continuous scaling down of the CMOS devices, the diameter of the contact plug is shrinking. It leads the plug resistance to increase, which is not desirable for high-performance transistor operation. With regards to 32nm CMOS devices and beyond, considerable work has been done to lower the contact resistance. From it, a Cu plug is thought to be a promising candidate [1,2]; however, a Cu plug may need a thick barrier layer to prevent diffusion to the source/drain junction. This means that most of the contact hole may be occupied by a barrier layer with high resistivity, which diminishes the advantage of Cu.

With respect to the conventional CVD-W plug, the diborane ($B_2H_6$)-reduction process for nucleation layer has been reported to lower the resistivity compared with the conventional silane ($SiH_4$) process [3], although its efficiency in a 32nm-node-size plug and the mechanism of the decrease have not been clarified yet.

In this paper, the authors show for the first time that a novel W plug process satisfies the resistance required for 32nm CMOS devices and beyond. The authors also discuss the origin of the low resistivity. Several analyses reveal that the plug resistance is determined by the amount of fluorine in the barrier metal and the grain size of the W film, rather than residual fluorine concentration or crystallinity of the W film.

## 2. Experimental

CVD-W films were deposited on MOCVD-TiN/PVD-Ti structures. Atomic layer deposition (ALD) technique was employed to form a nucleation layer. $B_2H_6$ and $SiH_4$ were used as the reducing agents in these depositions. This was followed by a bulk layer deposited by an identical and conventional CVD method, in which the reducing agent is $H_2$.

For the plug resistance measurement, a 65~45nm-node test element group (TEG) with varied contact hole size was used. Depth and bottom diameter of the plugs were typically 350nm and 50~90nm, respectively.

## 3. Results and discussion

*Resistivity reduction by employing $B_2H_6$*

At first, resistivity of the blanket W films was measured. A total thickness of 20~100nm was chosen to simulate the film in the plug, as the radius of the plug will be 20~30nm in a 32nm node and beyond. As W films have to be deposited on conductive TiN/Ti films, they were calculated by the equation

$$1/R_W = 1/R_{final} - 1/R_{initial}, \quad (1)$$

where $R_W$, $R_{final}$ and $R_{initial}$ represent sheet resistance of W film, W/TiN/Ti stacked film and TiN/Ti stacked film, respectively. It should be noted that a constant resistance of TiN/Ti film is assumed in the equation (1). Therefore, degradation of the TiN/Ti barrier layer by $WF_6$ gas attack appears as an increase of $R_W$.

Film thickness dependence of the resistivity using $SiH_4$- or $B_2H_6$-reduction process is shown in Fig. 1. It is seen that W film on $B_2H_6$-reduced nucleation layer has ~15% lower resistivity for the entire region in this figure, indicating the advantage of the process for 32nm devices and beyond.

Figure 2 shows the Kelvin resistance of the plugs on NMOS with $SiH_4$- and $B_2H_6$-reduction processes using a 65nm-node TEG. Due to the low resistivity shown in Fig. 1, plug resistance is effectively decreased.

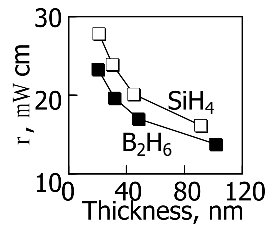



Fig. 1 Thickness dependence of the measured resistivity of W films.

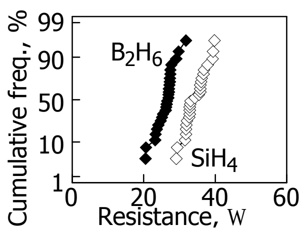



Fig. 2 Kelvin resistance of the W films with $B_2H_6$- and $SiH_4$- reduced nucleation layers on NMOS.

Figure 3 shows the hole-size dependence of the median value of a 300nm-height plug resistance on NMOS. With optimized barrier and nucleation processes, a resistance of ~50Ω in ~50nm-$f$ plug is achieved. This result satisfies the resistivity requirement for 32nm CMOS devices without employing a Cu plug process.

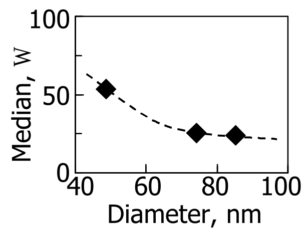



Fig. 3 Plug diameter dependence of the Kelvin resistance of $B_2H_6$- nucleated samples under optimized processes.

*Origin of the low resistivity*

To investigate the origin of the low resistivity of $B_2H_6$-reduced samples, several models were considered.

*Model 1:* The bulk film may contain less fluorine, as is the case in the nucleation layer [3].

*Model 2:* It is known that if the process is inadequate,

$WF_6$ attacks the barrier and fails the contact. This undesirable reaction may be decreased when $B_2H_6$ is employed.

*Model 3:* $B_2H_6$-reduced films may have larger grains.

*Model 4:* The film may have better crystallinity, although the $B_2H_6$ nucleation layer is said to be amorphous.

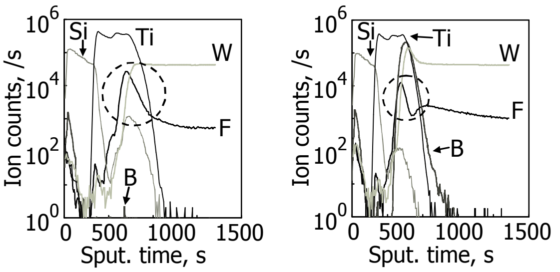
To test these items, the following experiments were performed.

*(1) SIMS analysis.* To examine Models 1 and 2, back-side SIMS analyses were performed. Figure 4 shows the results on the $SiH_4$- and $B_2H_6$-reduced films. Comparing the profile of the $B_2H_6$ sample with that of the $SiH_4$ sample, the following differences are found:

**1.** The nucleation layer contains a large amount of boron. W-B compound may be formed in this layer, as the boron profile effects the intensity of the matrix (W).

**2.** The nucleation layer contains less fluorine and penetration of fluorine into the TiN/Ti barrier is suppressed (indicated by the circle). This result supports Model 2.

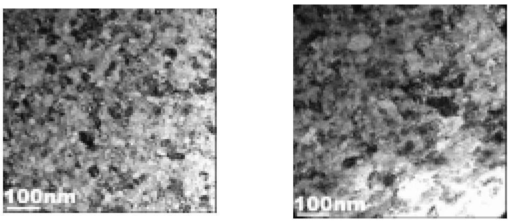
**3.** On the other hand, bulk layer is found to contain more fluorine. This result indicates that Model 1 is not accurate regarding the bulk layer.




(A) $SiH_4$ (B) $B_2H_6$

Fig. 4 Back-side SIMS profiles of $SiH_4$- and $B_2H_6$- reduced samples.

*(2) Surface TEM inspection.* To examine Model 3, grain size of the samples was measured by a surface TEM micrograph. After ~200nm deposition, W films were polished down to ~50nm. Figure 5 shows the results. It is seen that the horizontal grain size with the $B_2H_6$ process is larger than with $SiH_4$. Their measured grain sizes are 43nm and 24nm, respectively.




(A) $SiH_4$ (B) $B_2H_6$

Fig. 5 Surface TEM micrograph of $SiH_4$- and $B_2H_6$- reduced samples. The grain sizes were measured to be 24nm and 43nm, respectively.

Resistivity increase due to the grain boundary scattering can be calculated by the equation [4]

$$r_0/r = 1-(3/2)g + 3g^2 - 3g^3 \ln(1+1/g), \quad (2)$$

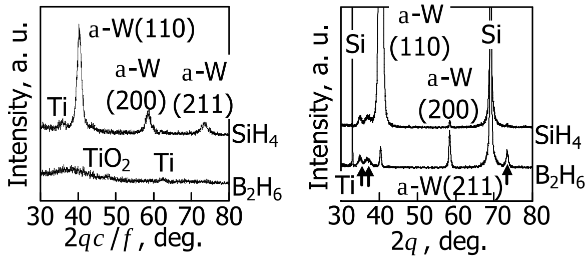
where $r$ and $r_0$ represent resistivity of the film and bulk W, respectively. $g$ is given by

$$g = \frac{l_0}{G}\frac{R}{1-R}, \quad (3)$$

where $l_0$, $G$ and $R$ denote mean free path of electrons in bulk W, grain size of the film and the electron reflection coefficient of the boundaries, respectively. Assuming that $l_0$=41nm [5] and $R$=0.5, $B_2H_6$ film was calculated to have ~30% lower resistivity than the $SiH_4$ film.

These results support the model 3, although the difference is larger than the results in Fig. 1.

*(3) X-ray diffraction.* To estimate the degree of crystallization, X-ray diffraction (XRD) was measured. The results are shown in Fig. 6. Compared with the $SiH_4$ sample, the $B_2H_6$ sample has different and very weak peaks. This result does not support Model 4.




(A) Nucleation film (B) Total film

Fig. 6 XRD spectra of the films. (A) In-plane spectra of nucleation layers; (B) Out-of-plane spectra of total films.

In summary, the origin of the lower resistivity of $B_2H_6$ samples compared to $SiH_4$ samples is thought to be determined by the amount of the penetrated fluorine to the barrier and the grain size of W film, as are revealed in SIMS and TEM results. Owing to these improvements, a resistance of ~50Ω in ~50nm-$f$ plug is achieved, although the higher fluorine content in the bulk W film shown in the SIMS profiles may lead the periodicity of the W atoms in the crystals to disturb, as appeared in XRD results, thereby increasing the resistivity.

## 4. Conclusion

The effect of employing $B_2H_6$ in a W-ALD nucleation layer on the contact resistance has been presented. A low resistance of ~50 ohms in a 32nm-node contact with a diameter of ~50nm is achieved through optimized barrier and nucleation processes. This result shows that the resistance value required for 32nm CMOS devices can be successfully satisfied without employing a Cu plug process.

Based on several analyses, it has also been revealed that the plug resistance is determined by the amount of fluorine in the barrier metal and the grain size of the W film.

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