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Spin Transfer Torque RAM (STT-RAM) Technology

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Spin-transfer torque (STT) writing technology [1], combined with the newly-observed high tunneling magnetoresistance (TMR) of greater than 300% in magnetic tunnel junctions (MTJs) with magnesium oxide (MgO) tunnel barriers [2], provides a practical path to the realization of gigabit-scale STT-RAM (Spin-Transfer Torque RAM) with low power consumption, fast operation speed (few nanoseconds), and excellent scalability to future semiconductor nodes. STT-RAM retains all the benefits of first-generation, field-switched MRAM (Magnetic RAM), such as non-volatility and fast, symmetrical read and write speeds, while overcoming all the hurdles, such as high write current and poor scalability. The attributes of STT-RAM are attractive for replacing not only existing non-volatile memory products, but also SRAM and DRAM, in wireless and embedded applications. The tunable resistance, large signal, and high spin polarization in MTJs with MgO tunnel barriers enable both ultrafast reading and low switching current in memory applications. We have previously reported that the intrinsic STT switching current density J_{c0} can be 2–3 MA/cm^2 for bottom pinned MTJ structures with a single MgO tunnel barrier [3], and that J_{c0} can be further reduced to less than 1 MA/cm^2 in dual MTJ structures with two MgO tunnel barrier layers and two oppositely oriented pinned layers on both sides of the free layer [4,5]. At the 45 nm technology node, this corresponds to an STT switching current of less than 40 μA. In this paper, we will focus on STT switching results obtained from bottom pinned and dual MgO MTJ bit-cells in the nanosecond regime.

The STT-RAM memory cell with integrated CMOS transistor is shown in Figure 1. Its smaller write current, simpler architecture, and similar manufacturing process compared with first-generation MRAM results in a cell area that can be as small as 6 F^2 for single-level STT-RAM. Multi-level STT-RAM cells can be even smaller [6]. Typical *I*–*V* and *R*–*V* switching curves of bottom pinned MgO MTJs with TMR signals of approximately 150% are shown in Figure 2, while the STT switching current in the nanosecond regime is shown in Figure 3. For a pulse width of 5 ns and an MTJ having dimensions of 115 × 180 nm^2, the STT switching current I_c is approximately 260 μA, which corresponds to a switching current density of 1.6 MA/cm^2. Figure 4 shows that the STT switching voltage distribution of a single cell having a coercivity of 150 Oe can be as small as 2.1% (1σ) at a pulse width of 15 ns. In fact, this switching voltage distribution remains essentially unchanged down to pulse widths of at least 2.5 ns, confirming that STT-RAM has adequate operating margin at read and write speeds of a few nanoseconds. In terms of reliability, the key issue for STT-RAM is the breakdown characteristic of the MgO tunnel barrier. Figure 5 shows that the breakdown voltage in the nanosecond regime is more than 3 times greater than typical STT switching voltages, which significantly increases the margin between switching voltage and breakdown in the STT-RAM operating range. Furthermore, an endurance stress test at 10 ns pulse width and 1.0 V stress voltage shows negligible change in signal output after more than 4×10^{12} write cycles, as shown in Figure 6. The endurance test was suspended due to test time, and longer tests are in progress. Details of the techniques involved in reducing the STT switching current and achieving consistent switching in the nanosecond regime will be presented and discussed. The key advantages of STT writing technology and the technical issues involved in commercializing STT-RAM will also be highlighted. Finally, the potential applications of STT-RAM in mobile devices, digital consumer electronics and automotive products will be outlined.

References

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[4] Y. Huai, et al., Appl. Phys. Lett. **87**, 222510 (2005); Z. Diao, et al., Appl. Phys. Lett. **90**, 132508 (2007).
[5] Grandis U.S. patents 6958927, 7057921 and 7088609.
[6] Grandis U.S. patent 6985385.

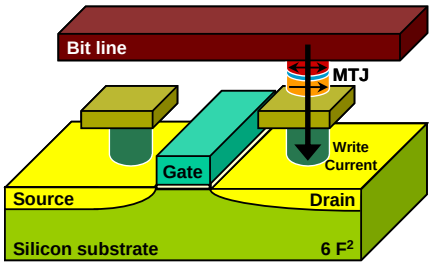

Figure 1. STT-RAM cell with integrated CMOS transistor. The area of a single-level STT-RAM cell can be as small as 6 F^2.

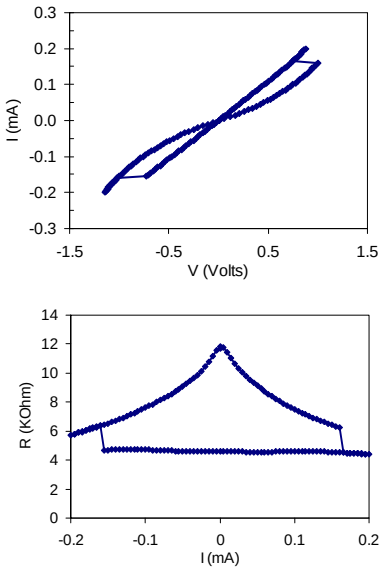

Figure 2. Typical I–V and R–I curves of current-switched, bottom pinned MgO MTJs with TMR signals of 150%.

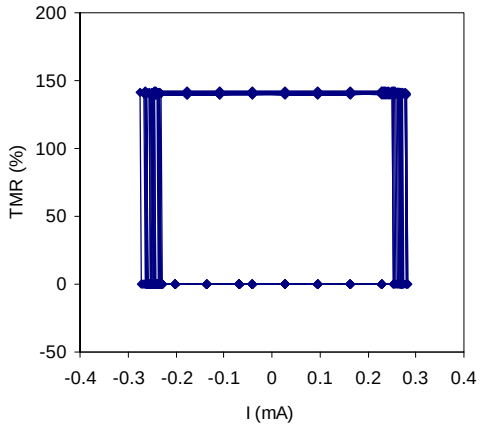

Figure 3. Repeated STT switching loops for a bottom pinned MgO MTJ. The pulse width is 5 ns and the MTJ dimensions are 115 × 180 nm^2.

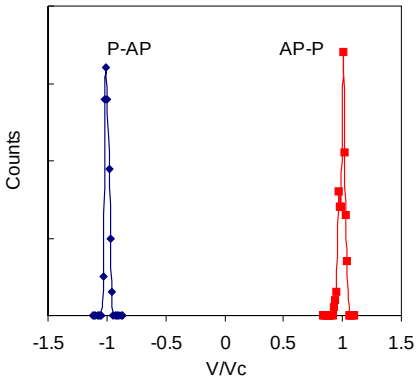

Figure 4. STT switching voltage distribution of a single cell having a coercivity of 150 Oe. The pulse width is 15 ns and the sigma is 2.1%.

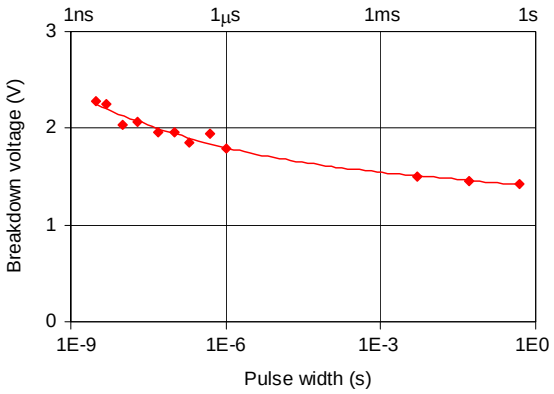

Figure 5. Breakdown voltage versus pulse width. For 10 ns pulses, the breakdown voltage is more than 3 times greater than typical STT switching voltages.

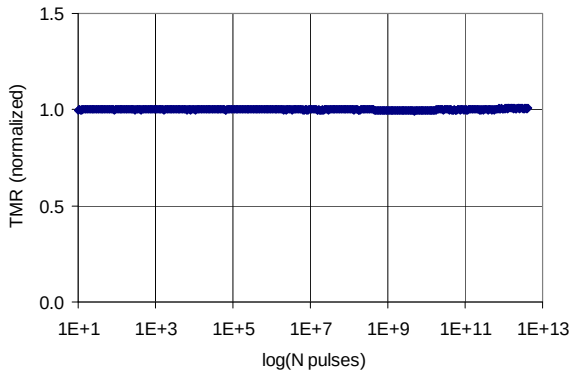

Figure 6. Endurance stress test. The pulse width is 10 ns and the stress voltage is 1.0 V. The test was suspended due to test time.