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The Magnetic Racetrack Memory: a novel spintronic device based on the current induced motion of domain walls

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1. Introduction

There are two main means of storing digital information for computing applications: in the form of solid state random access memories (RAM) or in the form of magnetic hard disk drives (HDDs). Both classes of devices are evolving at a very rapid pace but currently, as has been the case for the past many years, the cost of storing a single data bit in an HDD is approximately 100 times cheaper than in a solid state RAM. While the low cost of storing data in an HDD is very attractive, these devices are intrinsically slow, with typical access times of several milliseconds due to the large mass of the rotating disk, and are unreliable, with a significant chance of complete loss of all data in the HDD due to the possibility of mechanical interaction of the recording head and disk. RAM, on the other hand can be very fast and highly reliable, as in SRAM and DRAM technologies. Computing systems could be vastly simplified if there was a single memory-storage device which had the low cost of the HDD but the high performance and reliability of solid state memory.

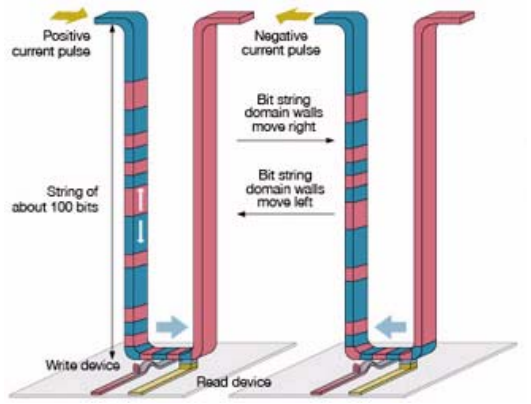

Fig. 1 Schematic illustration of the race-track memory showing a series of magnetic domain walls propagating around the racetrack driven by a sequence of current pulses [1].

2. Racetrack Memory

Since both silicon based microelectronic devices and HDDs are essentially two-dimensional technologies, containing, two dimensional arrays of transistors and magnetic bits, respectively, the conventional means of developing cheaper memory and storage devices relies on reducing the size of individual memory elements or data storage bits. An alternative, perhaps more radical approach, is to consider constructing truly three-dimensional devices. One such approach is the "Racetrack Memory" [1]. In this *storage-class memory device* magnetic domains are used to store information in tall columns of magnetic material arranged perpendicularly to the surface of a silicon wafer (see Figure 1). These columns comprise the magnetic racetracks. The magnetic domain walls are formed at the boundaries between magnetic regions magnetized in opposite directions (i.e. up or down) along a racetrack. Each magnetic region has a "head" (positive or north pole) and a "tail" (negative or south pole). Successive domain walls along the racetrack will alternate between "head to head" and "tail to tail" configurations. If a magnetic field is used to move these domain walls then neighbouring walls will move in opposite directions and will eventually annihilate each other. Magnetic memory devices using domain walls were studied intensively several decades ago but all of these devices manipulated domain walls by applying magnetic fields [2,3], thereby limiting the architecture of such devices.

In the Racetrack Memory the domain walls are moved up and down the race-track not by magnetic field but rather by nanosecond long current pulses using the phenomenon of spin momentum transfer [4]. When a current is passed through a magnetic material it becomes spin-polarized, due to spin-dependent diffusive scattering, and so carries spin-angular momentum. When the spin-polarized current is passed through a domain wall the current transfers spin angular momentum to the wall, thereby applying a torque to the moments in the domain wall which can result in motion of the wall [5-9]. When the magnetic columns are sufficiently narrow (<~100nm) the spin momentum transfer interaction of the current with the domain wall will dominate over the self-field of the current. Thus, the racetracks are composed of columns of magnetic material approximately one hundred nanometers in diameter and several tens of microns tall, thereby accommodating up to 100 domain walls per racetrack.

The cost of storing one data bit in the racetrack memory is lowered the greater the number of domain walls which are stored in an individual racetrack. Each racetrack has an associated reading and writing element (see Figure 1). The domain walls in the magnetic race-track are read using magnetic tunnel junction magnetoeresistive sensing devices arranged in the silicon substrate and can be written using a variety of schemes [1].

3. Current induced domain wall motion

A series of experiments [5-9] which explore the current and field induced motion of domain walls (DWs) along permalloy nanowires will be discussed. The DW structure, whether vortex or transverse, and the DW chirality can be determined from the resistance of the DW. The current induced depinning of DWs from artificially created pinning

sites - notches along the edges of the nanowires- is shown to be surprisingly insensitive to the DW structure [2]. The velocity of domain walls driven by current alone in the absence of magnetic field, is shown to exceed 110 m/sec [3]. A number of studies which show the importance of the precessional nature of the DW motion will be presented [4,5]. In particular, we find that the probability of dislodging a domain wall, confined to a pinning site oscillates with the length of the current pulse, with a period of just a few nanoseconds [4]. This behaviour is connected to a current-induced oscillatory motion of the domain wall. When the current is turned off during phases of the domain wall motion when it has sufficient momentum, the domain wall is driven out of the confining potential in the opposite direction to the flow of spin angular momentum, a sort of *boomerang* effect.

3. Summary

The Racetrack Memory is a magnetic shift register which allows the storage of one to two orders of magnitude larger number of data bits in the same area of silicon in which conventional memory technologies store a single data bit. Thus, this three-dimensional technology is correspondingly one to two orders of magnitude cheaper. The Racetrack Memory promises a solid state memory with storage capacities and cost rivalling that of magnetic disk drives but with the high performance and reliability of conventional solid state memories. The Racetrack Memory is possible due to recent developments in spintronic materials and phenomena. Although the Racetrack Memory is in the early stages of its development, there are no obvious roadblocks to its eventual successful deployment. Its detailed performance and reliability characteristics will depend on future developments in the magnetic materials and structure of the racetrack and in progress in our detailed understanding of the physics of the current and field induced motion of domain walls.

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References

[1] S.S.P. Parkin, US Patents 6,834,005, 6,898,132, 6,920,062, 7,031,178, and 7,236,386 (2004-2007).
[2] Matick, R.E. “Computer storage systems and technology” (John Wiley & Sons, New York, 1977).
[3] Middelhoek, S., George, P.K. & Dekker, P. “Physics of Computer Memory Devices” (Academic Press, London, 1976).
[4] Slonczewski, J. *J. Magn. Magn. Mat.* **159**, L1 (1996).
[5] M. Hayashi, L. Thomas, C. Rettner, X. Jiang, R. Moriya and S.S.P. Parkin, Phys. Rev. Lett. **97,** 207205 (2006).
[6] M. Hayashi, L. Thomas, Y. Bazaliy, C. Rettner, R. Moriya, X. Jiang and S.S.P. Parkin, Phys. Rev. Lett. **96,** 197207 (2006) and M. Hayashi, L. Thomas, C. Rettner, R. Moriya, Y. B. Bazaliy, & S.S.P. Parkin, Phys. Rev. Lett. **98**, 037204 (2007).
[7] L. Thomas, M. Hayashi, X. Jiang, C. Rettner and S.S.P. Parkin, Nature 443, 197 (2006)
[8] L. Thomas, M. Hayashi, X. Jiang, R. Moriya, C. Rettner, and S.S.P. Parkin, Science **315**, 1553 (2007).
[9] M. Hayashi, L. Thomas, C. Rettner, R. Moriya, and S.S.P. Parkin, Nat. Phys. **3**, 21 (2007).