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A Small Area, 3-Dimensional On-chip Inductors for High-speed Signal Processing under Low Power Supply Voltages

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Abstract

Using fine-pitched ULSI local interconnects, an extra-small-area, 3-dimensional (3-D) solenoid-shaped inductor is developed for high-speed logic LSIs. The 3-D solenoid inductor has 4-layered solenoid structure of the local interconnects, achieving 85% area reduction with smaller crosstalk-noise than a conventional monolayer spiral inductor using wide global interconnects. The 3-D solenoid structure has higher self-resonant frequency than a stacked spiral inductor due to the small effective parasitic capacitance. A 20 Gb/s D-type flip-flop (D-F/F) with the 3-D solenoid inductor is confirmed to have smaller jitter than that with the monolayer spiral one under V_{DD}=1V.

Introduction

For high-speed data communication over several Gb/s, high-speed logic circuits such as SerDes (Serializer/ Deserializer) require higher clock frequency than the toggle frequency in the conventional CMOS logic (Fig. 1). Inductor peaking technique is used to realize the high-speed logic, however, conventional inductor used wide-pitched global lines, enlarging the inductor area, or eventually the chip area. Therefore, inductors should be miniaturized with suppressing crosstalk-noise between adjacent ones.

We have developed an extra-small-area, 3-dimensional solenoid-shaped (3-D solenoid) inductor using local Cu-interconnects, achieving 85% area reduction with smaller crosstalk-noise than a conventional monolayer spiral inductor. By the solenoid structure, 30% reduction in the parasitic capacitance was achieved referred to the stacked spiral inductor. Feasibility of the 3-D solenoid inductor is confirmed in a 20 Gb/s D-type flip-flop with V_{DD}=1V.

Characteristics of the small-area 3-D solenoid inductor

A 90 nm-node CMOS process with 5-layered local Cu-interconnects (M1-M5) and a global Cu one (M6) was used for three types of inductors with ~3nH, such as (1) a conventional monolayer spiral inductor in the M6 layer, (2) a multi-layer stacked spiral inductor [1] in the M2~M5 layers and (3) a 3-D solenoid inductor in the M2~M5 layers. The chip areas of both the stacked spiral inductor and the 3-D solenoid one were 85% smaller than that of the monolayer one (Fig. 2).

To obtain acceptable series resistance with tolerance to the electro-migration, the stacked spiral inductor and the 3-D solenoid were fabricated with 1μm-wide local Cu lines (Fig. 3). Therefore, the vertical inter-metal capacitance (C_v) was larger than the horizontal capacitance (C_h). In case of the stacked spiral inductor (Fig. 4(a)), the largest capacitance C_{v1} (between upper-outer and lower-outer metal) was loaded between input and output ports of the inductor, increasing the effective parasitic capacitance. In case of the 3-D solenoid inductor (Fig. 4(b)), the C_{v1} was loaded between the input port and the vicinity middle node, suppressing the effective parasitic capacitance [2].

Fig. 5 shows measured (a) the series inductance, (b) the series resistance and (c) the Q-factor of each inductor. Due to the small parasitic capacitance, the self-resonant frequency (f_{SR}) of the 3-D solenoid inductor was enlarged refer to that of the stacked spiral one (Fig. 5 (a)). The series resistance of both the local inductors were larger than that of the monolayer spiral one in global layer (Fig. 5 (b)) due to difference of the metal thicknesses (M6: 0.9 μm-thick and M2~M5: 0.3 μm-thick), lowering their Q-factors (Fig. 5 (c)). The lower Q-factor of the 3-D inductor, however, is not disadvantage for the peaking inductor, because series resistances are connected to the inductors (Fig. 1).

Table I lists the equivalent circuit parameters of each inductor extracted from the π-type circuit model (Fig. 6). It is confirmed that the parasitic capacitance of the 3-D solenoid inductor between the input and output ports (C_{int}) was 30% smaller than that of the stacked spiral inductor.

Crosstalk-noise between adjacent inductors

A crosstalk-noise between adjacent inductors was investigated (Fig. 7). Here, the distance between adjacent inductors was fixed as 10 μm, and the ports 1-2 and 3-4 were assigned to primary and secondary inductors, respectively. The absolute values of the measured S_{31} and S_{41} correspond to the crosstalk-noise between the adjacent inductors. The crosstalk-noise of the 3-D solenoid inductor was smaller than that of the monolayer inductor due to the small size. The crosstalk-noise was further suppressed by applying guard ring (GR) fabricated with metal-1 and p^+ diffusion layer.

D-F/F using 3-D solenoid inductor

To demonstrate performance of the 3-D solenoid inductor, D-type flip-flops (D-F/Fs) were fabricated with 90 nm-node CMOS process with 1V power supply. In this work, 0.4 and 0.7 nH 3-D solenoid inductors with 2 μm line width were used for the peaking inductors. Fig. 8 (a) shows a schematic diagram of the latch circuit using 2 peaking inductors [3]. Actually, including latch, I/O buffers and clock buffers, 23 inductors were used in the D-F/F. A D-F/F with conventional monolayer spiral inductors was also fabricated as a reference. The output eye diagrams of the data rate of 20 Gb/s had clear eye opening with small jitter for D-F/F with the 3-D solenoid inductors than that with the monolayer inductors (Fig. 8 (b) and (c)), while the inductor areas were reduced by 84 ~ 90%.

Conclusions

Extra-small-area, 3-D solenoid inductor using the local interconnects was developed for scaled down high-speed logic LSIs. The inductor area was 85% smaller than that of the monolayer inductor, suppressing the crosstalk-noise between the adjacent inductors. The feasibility for high-speed logic LSIs was confirmed by the 20 Gb/s D-F/F under 1 V power supply. The 3-D solenoid inductor is a key element for scaled-down high-speed logic LSIs with low power supply voltage.

References

[1] A. Zolfaghari et al., JSSC vol. 36, No. 4, 620 (2001)
[2] Chih-Chun Tang et al., JSSC vol. 37, No. 4, 471 (2002)
[3] Y. Amamiya et al., 2003 GaAs IC Symp. Dig., 169 (2003)

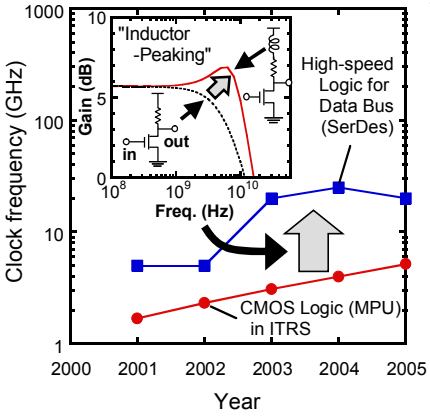

Fig. 1 Technology trend of the clock frequency. Inductor peaking is needed for high-speed logic (SerDes).

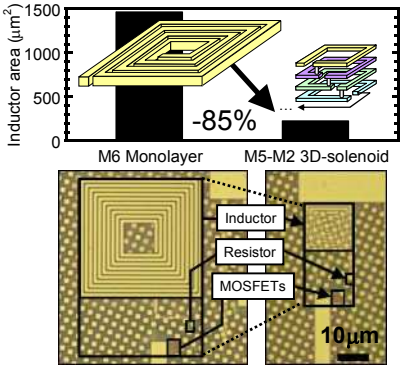

Fig. 2 Impact of the 3-D solenoid inductor on the chip area. The 3-D inductor composed of 4-layered local interconnects, while the conventional monolayer spiral one used the top-layered global interconnect.

Table I Structural parameters and equivalent circuit parameters of the inductors.

	Monolayer spiral	Stacked spiral	3-D solenoid
Metal layer	Metal-6 (global)	Metal-5~2 (local)	Metal-5~2 (local)
Chip Area	1464μm²	225μm²	225μm²
Metal thickness	0.9 μm	0.3 μm	0.3 μm
Inner-diameter	10 μm	1 μm	1 μm
Line width	1 μm	1 μm	1 μm
Space	0.4 μm	0.2 μm	0.2 μm
Turns	10	6	6
R_{met}	25.1 Ω	67.5 Ω	70.1 Ω
L_{met}	2.88 nH	3.15 nH	3.05 nH
C_{int}	3.5 fF	8.0 fF	5.5 fF

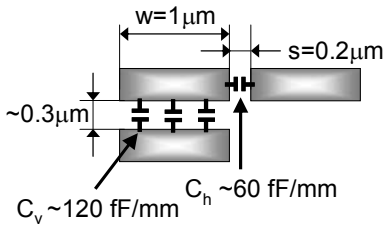

Fig. 3 Inter-metal capacitances of the multilayer inductor. Subscripts "v" and "h" correspond to vertical and horizontal, respectively.

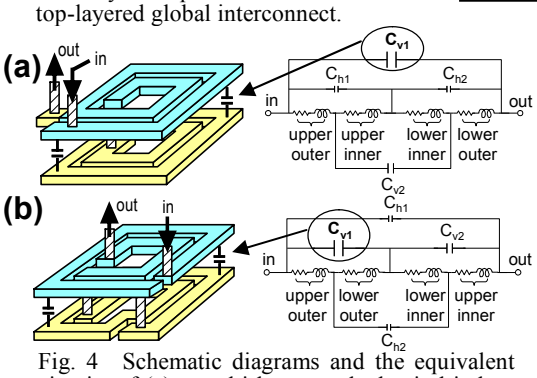

Fig. 4 Schematic diagrams and the equivalent circuits of (a) a multi-layer stacked spiral inductor and (b) a 3-D solenoid inductor.

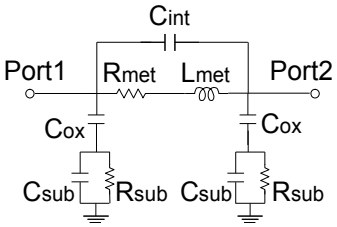

Fig. 6 Equivalent circuit of the on-chip inductors.

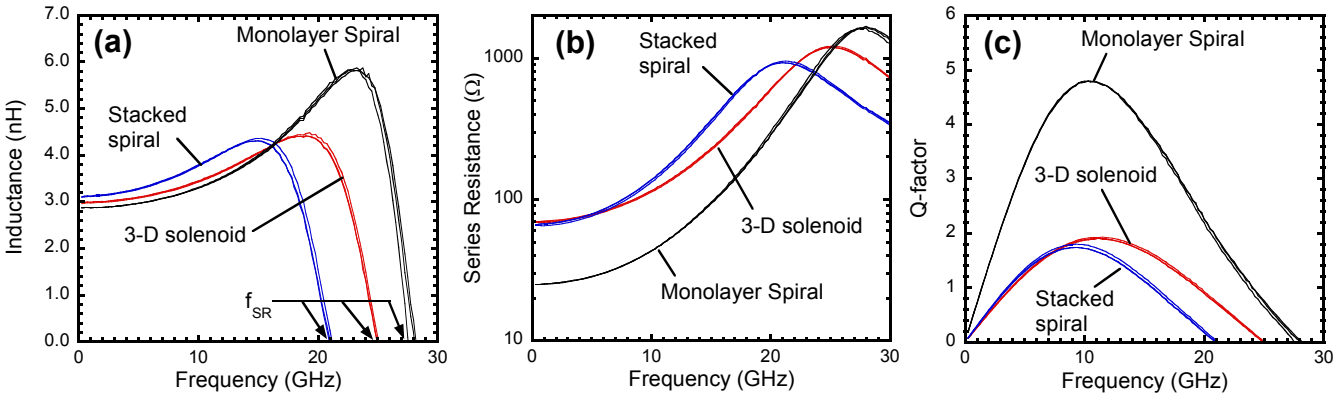

Fig. 5 Characteristics of the inductors; (a): Inductance, (b): Series resistance and (c) Q-factor.

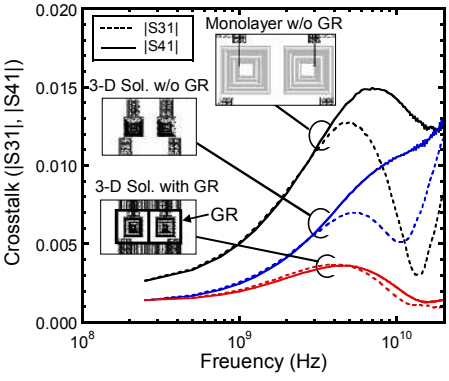

Fig. 7 Measured S-parameters (crosstalk-noise) of the adjacent inductors.

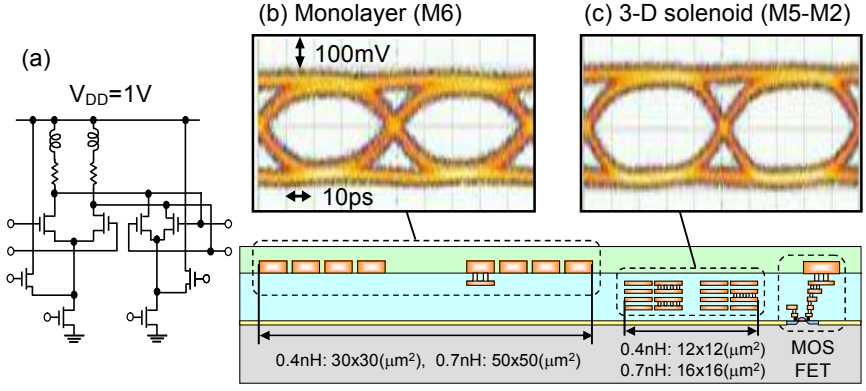

Fig. 8 D-F/F fabricated with 90 nm CMOS process; (a) Latch circuit diagram[3], Output eye diagrams of the D-F/Fs with (b) the conventional monolayer inductors and (c) the 3-D solenoid ones. The data rate was 20 Gb/s with V_{DD}=1 V.