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Wiring technology for analog and mixed signal LSIs

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1. Introduction

Wiring technology has been used to interconnect between transistors for digital LSIs, and expand the application area to analog and mixed signal LSIs.

This paper reviews the role of wiring and required condition for some important applications.

2. CMOS RF technology

Digital wireless communication technology emerged during 1990's and the market of cellular phones has become almost the same as or larger than that of the personal computer. CMOS technology had not been regarded as a more suitable device for RF applications than bipolar technology in 1990's, however technology scaling has increased the cutoff frequency up high enough for GHz frequency signal processing. After the year 2000; beginning with wireless networking chips, followed by cellular phone chips have used CMOS technology. CMOS process had to be addressed to realize high Q inductors. The quality factor Q of inductors affect the fundamental performance of RF circuits.

Phase noise S and current consumption I of LC oscillators which is one of the most important performance factors in wireless systems, have the following relations with Q of inductor.

$$ I_{osc} \propto \frac{1}{Q} \qquad S_\phi \propto \frac{1}{Q^2} $$

Thus increase of Q is the first priority of oscillator design. The Q of inductor is defined as;

$$ Q(\omega) = \frac{1}{2\pi} \cdot \frac{E_{magnetic} - E_{electric}}{E_{loss/cycle}} $$

Thus to increase Q, increase of inductance and substrate resistance and decrease of parasitic capacitance and series resistance are needed. Conventionally thicker metal, far from the substrate and neighboring metals, and a highly resistive substrate are effective, as shown in figure 1.

The thicker third layer metal attains a higher Q of 8 compared with thinner metal and the thicker 5th layer
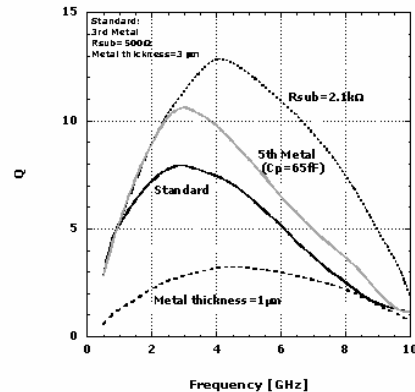

Fig. 1. Characteristic of inductor Q.

metal increases Q up to 11. Higher resistive substrate increases Q even further.

This condition is just the same as the condition for high quality global interconnects. Conventional Q of on chip inductor is less than 10 and an inductor of which the thickness is greater than several um and formed on a passivation film is used to obtain higher Q.

Another issue of the inductor is the large occupied area. Figure 2 compares chip area and chip cost of mixed signal SoCs for several design rules normalized by 0.35 um technology [1]. If an occupied area of analog circuits can't be scaled, the total cost will increase even if the area of digital circuits is scaled by decreasing the design rule.
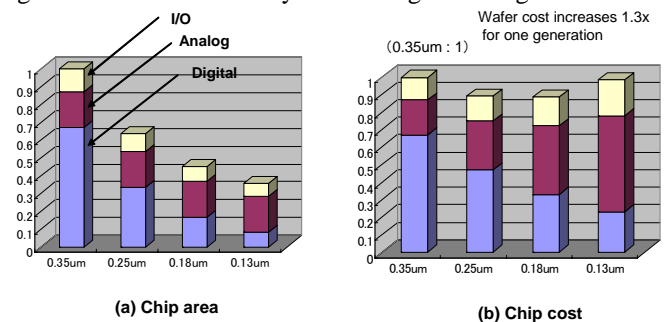

Fig. 2. Chip area and cost of mixed signal SoC [1].

A use of inductor to form resonators is effective to reduce noise power, to separate wanted signal from unwanted signals, and increase signal power. Thus conventional RF circuits use many inductors. However recent RF LSIs decrease the number of inductors [2]. One reason is to reduce occupied area and the other reason is

to address wide frequency range such as UWB and multi-band radio. An oscillator still needs inductor to reduce phase noise, however almost all RF circuits can be designed without inductors. The performance without inductor decreases a little however the chip cost can be decreased remarkably.

3. Millimeter wave SoCs and proximity data links

The frequency range used in current wireless systems is less than 5 GHz, however 60 GHz will be used for future millimeter wave communication. Millimeter wave communication is suitable for short distance broadband communication such as in-room communication between a tuner and a display in HDTV systems. Device size can be scaled and data rate can be increased up to several Gbps. Small size of inductor and/or transmission line will be used to realize impedance matching, resonators, and filters. The size of transmission line becomes feasible on IC technology when signal frequency is 60 GHz corresponding to a wavelength of about 2.5 mm.
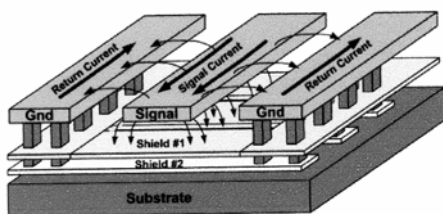

Fig. 3. A coplanar transmission line [3].

The structure of transmission line should be designed so as to minimize the energy loss at high frequency. One large loss occurs in silicon substrate. Some shielding techniques should be applied as shown in figure 3 [3].

Another interesting technology for millimeter wave application is on-chip antennas. Antennas can be integrated on a chip and this means all needed components for wireless systems can be integrated on a chip.

Figure 4 shows one example of the on-chip antenna [4]. Four antennas are integrated to form the phased-array system. The phased-array system can change the radiation pattern and realize beam forming to separate channels by controlling signal phases of each transmission signal to the antennas. Applications for millimeter wave technology will open new vistas for silicon integrated technology.
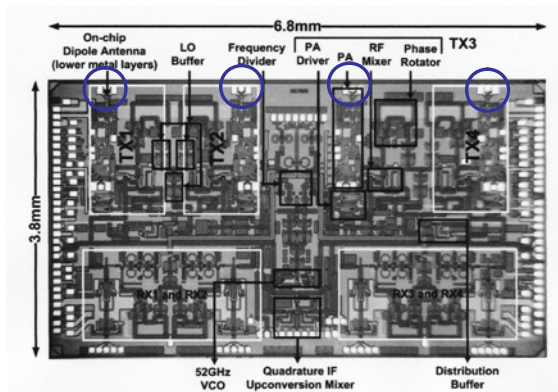

Fig. 4. On-chip antennas on a millimeter chip [4].

Another use of the inductor is for inductive coupling for high speed data link to realize proximity data transmission between chips as shown in figure 5 [5]. 3D integration needs high density, high speed, and low power data transmission techniques. The inductive coupling link can realize high speed data transfer to stacked chips. Furthermore the ESD protection circuit is not required in contrast to the conventional metal to metal contact. An ultra high speed data rate of Tbps with ultra low energy has been reported.
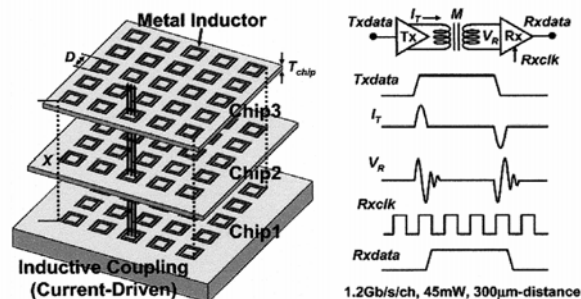

Fig. 5. Inductive coupling high speed data link [5].

4. Micro power systems

High speed data transfer has been realized; however electrical power transfer and control will become more important for real system integration. An adaptive V_{dd} control is needed for current SoCs to reduce power dissipation. External DC-DC converters are used for current SoCs, however on-chip distributed DC-DC converters are more effective than fine-grained adaptive controllers for each circuit block.

High Q and compact inductors and high density capacitors are required. Conventional inductance used for DC-DC converter is too large to be embedded on a chip. However higher operating frequency with introduction of high permeability materials can reduce the occupied area of inductors [6]. A coupling factor of 0.98, L/R ratio of 50 ns, and an efficiency of 85% have been obtained with wire width of 8 um and wire thickness of 1.25 um.

References

[1] A. Matsuzawa, IEICE, Tran. on Electronics, pp. 867-877, E87-C[6], 2004.

[2] R. B. Staszewski, et. al., IEEE, Journal of Solid-State Circuits., Vol.39, No. 12, pp. 2278-2290, Dec. 2004.

[3] A. Natarajan, et. al., IEEE, Journal of Solid-State Circuits, Vol. 40, No. 12, pp. 2502-2514, Dec. 2005.

[4] A. Natarajan, et. al., IEEE, Journal of Solid-State Circuits, Vol. 41, No. 12, pp. 2807-2819, Dec. 2006.

[5] N. Miura, et. al., IEEE, Journal of Solid-State Circuits, Vol. 41, No. 1, pp. 23-34, Jan. 2006.

[6] G. Schrom, et. al., Proc. ISLPED'04, pp. 263-268, 2004.